

# Cascade Three-Level AC/AC Direct Converter

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**Abstract**—This paper proposes a novel family of cascade three-level (TL) ac–ac direct converters based on ac switch cells, which transfer unsteady high ac voltage with distortion into regulated sinusoidal voltage with low total harmonic distortion (THD). The topological family includes buck TL–boost, buck–boost TL, and buck TL–boost TL modes. In order to achieve a reliable TL ac–ac conversion, a double transient voltage feedback control strategy of the output voltage and the voltage across the flying capacitor is introduced in this paper. A 500-VA 220-V  $\pm 10\%$  50-Hz ac/220-V 50-Hz ac prototype is presented with the experimental results to prove that the converters have four improved advantages simultaneously, including lower voltage across power switches, bidirectional power flow, low THD of output voltage, and higher input power factor.

**Index Terms**—AC switch cell, ac–ac direct converter, double transient voltage feedback control, three-level (TL).

## I. INTRODUCTION

THE ac–ac converters have been widely used in various industrial domains in recent years. However, recent research on the ac–ac converter technology mainly focuses on two-level ac–ac converters and ac–dc–ac-type multilevel ac–ac converters [1]–[4]. The former includes ac–ac converters with electrical isolation and the ones without any electrical isolation such as ac choppers, thyristor phase-controlled cycloconverters, or matrix converters. The latter includes ac–ac converters with no electrical isolation as well as the ones with low or middle frequency electrical isolation.

Nowadays, the ac–ac converters are required not only for the low-voltage but also for the high-voltage input applications. In these fields, a multilevel technique is effective to reduce the voltage across power switches with improved output voltage. A multilevel technique was firstly proposed in inverters [5]–[13] and then developed in dc–dc converters and rectifiers [14]–[17]. So far, a multilevel technique used in ac–ac converters has been mainly limited to ac–dc–ac-type ac–ac converters, which have many shortcomings such as more power stages, unidirectional power flow, low input power factor, and weak adaptability to various loads [18], [19]. Therefore, a cascade three-level (TL)

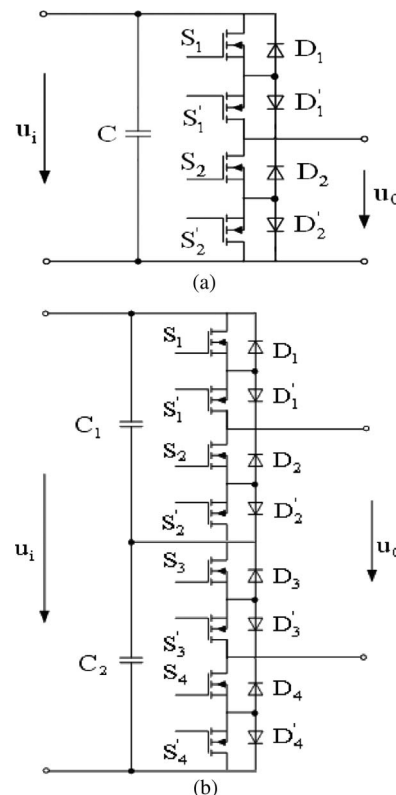


Fig. 1. AC switch cells. (a) Two-level ac switch cell. (b) TL ac switch cell.

ac–ac direct converter was proposed in order to improve the multilevel ac–ac converters [20].

This paper proposes a novel family of cascade TL ac–ac direct converters based on ac switch cells. In order to achieve a reliable TL ac–ac conversion, a strategy of the double transient voltage feedback control is presented also. The converters proposed in this paper have single-stage power conversion (low-frequency alternate-current LFAC-LFAC), bidirectional power flow, and higher input power factor compared with the ac–dc–ac-type TL ac–ac converters. Moreover, the converters have lower voltage across power switches compared with the two-level ac–ac converters. The converters are targeted to be used on a new type of regulated sinusoidal ac power supply, electronic transformer, and ac regulator in which high-voltage input (output) and/or bidirectional power flow are needed.

## II. CONVERTER TOPOLOGY

As shown in Fig. 1, two-level ( $u_i, 0$ ) and TL ( $u_i, u_i/2, 0$ ) ac switch cells are presented in this paper. A TL ac switch cell is produced by two-level ac switch cells in series.

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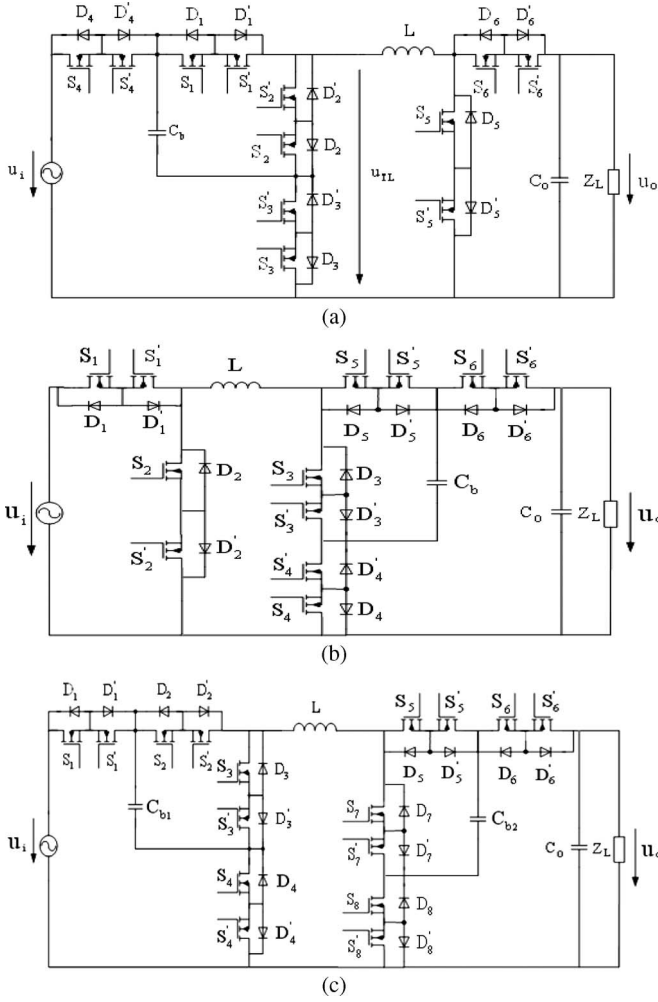


Fig. 2. Cascade TL ac-ac direct converter. (a) Buck TL-boost mode. (b) Buck-boost TL mode. (c) Buck TL-boost TL mode.

Based on ac switch cells, a novel family of cascade TL ac-ac direct converters shown in Fig. 2 is proposed. The topological family includes buck TL-boost, buck-boost TL, and buck TL-boost TL modes. According to different output voltages, pulsewidth modulation (PWM) controlled TL ac-ac converters chop in different operation modes with three voltage levels. Therefore, the converters can directly transfer unsteady high ac voltage with distortion into regulated sinusoidal voltage with low total harmonic distortion (THD).

### III. OPERATING PRINCIPLES

To simplify the steady-state analysis, the following assumptions are made: 1) Switching and conduction losses of the components are neglected; 2) input and output voltages are considered constant during one switching period  $T_s$ ; 3) parasitic parameters of inductor  $L$  for energy storage, flying capacitor  $C_b$ , and filter capacitor  $C_o$  are neglected; and 4) flying capacitor  $C_b$  is large enough to be considered as a constant dc voltage source with value  $u_i/2$ . According to the polarities of input voltage  $u_i$  and current of inductor  $L$  for energy storage  $i_L$ , the buck TL-boost mode cascade TL ac-ac direct converter can work in four kinds of operation modes: A ( $u_i > 0, i_L > 0$ ), B ( $u_i > 0, i_L < 0$ ), C ( $u_i < 0, i_L < 0$ ), and D ( $u_i < 0, i_L > 0$ ).

#### A. Operation Mode A

Power switches  $S_1 \sim S_6$  chop with high frequency, and power supply delivers power to the ac load. Topological states during one  $T_s$  in mode A are shown in Fig. 3.

State 1 [ $t_0 \sim t_1$ ] [refer to Fig. 3(a)]:  $S_2, S_4$ , and  $S_5$  are on.  $C_b$  and  $L$  are both charged by power supply, and voltage  $u_{TL} = u_i/2$ .  $C_o$  transfers power to the ac load. The voltage across  $L$  is  $u_L = u_i - u_{Cb}$ , so inductor current  $i_L$  increases linearly. The change of  $i_L$  is given by

$$\Delta i_1 = \int_{t_0}^{t_1} \frac{u_i - u_{Cb}}{L} dt = \frac{u_i - u_{Cb}}{L} (t_1 - t_0) = \frac{u_i}{2L} (t_1 - t_0). \quad (1)$$

State 2 [ $t_1 \sim t_2$ ] [refer to Fig. 3(b)]:  $S_1, S_4$ , and  $S_5$  are on.  $S_2$  is off.  $L$  is still charged by power supply, and  $u_{TL} = u_i$ .  $C_o$  delivers power to the ac load. Voltage  $u_L = u_i$ , so  $i_L$  still increases linearly. The change of  $i_L$  is obtained as

$$\Delta i_2 = \int_{t_1}^{t_2} \frac{u_i}{L} dt = \frac{u_i}{L} (t_2 - t_1). \quad (2)$$

State 3 [ $t_2 \sim t_3$ ] [refer to Fig. 3(c)]:  $S_1, S_3$ , and  $S_6$  are on.  $S_4$  and  $S_5$  are off.  $C_b$  and  $L$  transfer power to  $C_o$  and the ac load, and  $u_{TL} = u_i/2$ . Voltage  $u_L = u_{Cb} - u_o$ , so  $i_L$  starts to decrease linearly. The change of  $i_L$  can be given by the following:

$$\Delta i_3 = \int_{t_2}^{t_3} \frac{u_{Cb} - u_o}{L} dt = \frac{u_i/2 - u_o}{L} (t_3 - t_2). \quad (3)$$

State 4 [ $t_3 \sim t_4$ ] [refer to Fig. 3(d)]:  $S_2, S_3$ , and  $S_6$  are on.  $S_1$  is off.  $L$  supplies power to  $C_o$  and the ac load, and  $u_{TL} = 0$ . Voltage  $u_L = -u_o$ , so  $i_L$  still decreases linearly. The change of  $i_L$  is

$$\Delta i_4 = \int_{t_3}^{t_4} \frac{-u_o}{L} dt = \frac{-u_o}{L} (t_4 - t_3). \quad (4)$$

In the steady state, the change of  $i_L$  during one  $T_s$  must be zero, i.e.,  $\Delta i_1 + \Delta i_2 + \Delta i_3 + \Delta i_4 = 0$ . From (1)–(4), (5) is obtained as

$$u_i(t_1 - t_0)/2 + u_i(t_2 - t_1) + (u_i/2 - u_o)(t_3 - t_2) - u_o(t_4 - t_3) = 0. \quad (5)$$

Then, the ratio of the output root mean square (rms) voltage to the input rms voltage of the converter in continuous conduction mode is given by

$$\frac{U_o}{U_i} = \frac{(t_2 - t_0) + (t_3 - t_1)}{2[(t_4 - t_0) - (t_2 - t_0)]} = \frac{D + D'}{2(1 - D)} \quad (6)$$

where  $D = (t_2 - t_0)/(t_4 - t_0)$  is the duty cycle of  $S_4, S_5$  ( $S'_4, S'_5$ ) and  $D' = (t_3 - t_1)/(t_4 - t_0)$  is the duty cycle of  $S_1$  ( $S'_1$ ).

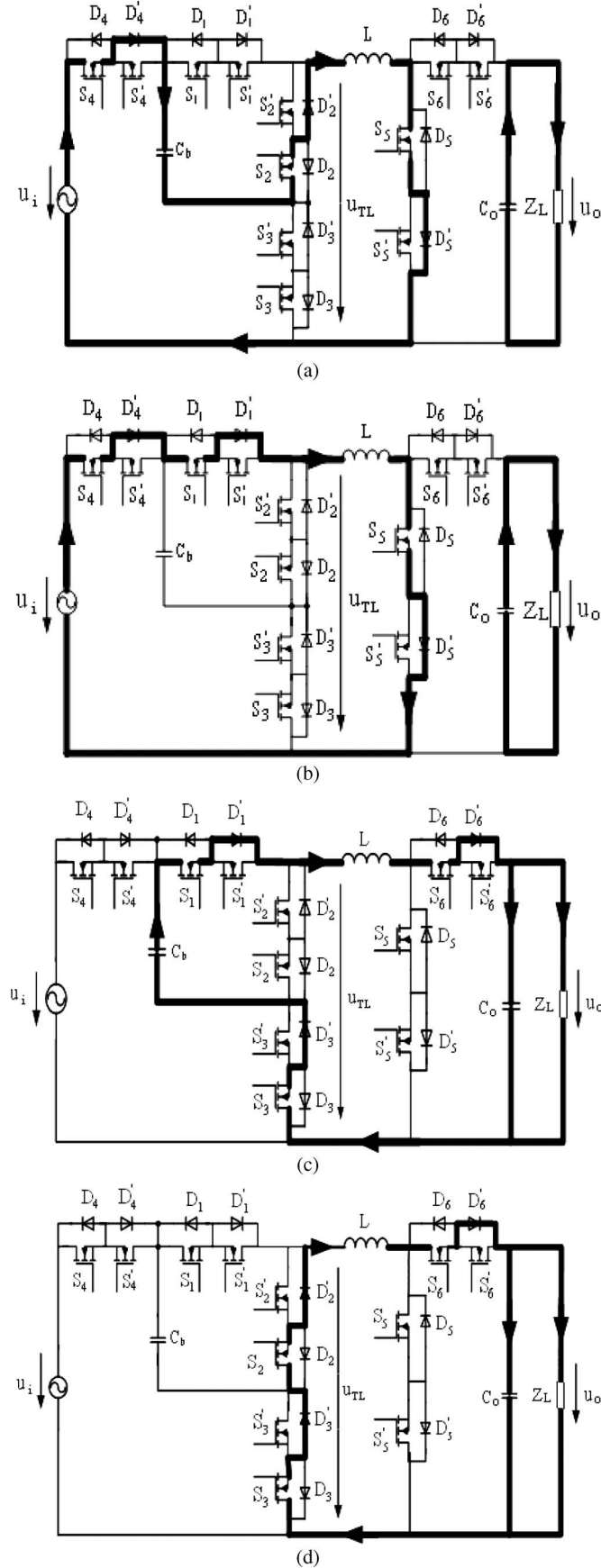


Fig. 3. Topological states during one switching period  $T_s$  in mode A. (a) State 1  $[t_0 \sim t_1]$ . (b) State 2  $[t_1 \sim t_2]$ . (c) State 3  $[t_2 \sim t_3]$ . (d) State 4  $[t_3 \sim t_4]$ .

### B. Operation Mode B

Power switches  $S'_1 \sim S'_6$  chop with high frequency, and the load delivers power to the power supply. Voltage  $u_{TL}$  varies with  $u_i/2$ ,  $u_i$ ,  $u_i/2$ , and 0. Topological states during one  $T_s$  in mode B are shown in Fig. 4. Operation modes C and D are similar to A and B, respectively, and we do not provide detailed analysis in this paper.

## IV. DESIGN CONSIDERATIONS

Design specifications of the buck TL-boost mode cascade TL ac-ac direct converter are defined as follows: input voltage  $U_i = 198\text{--}242$  V (50 Hz) ac, output voltage  $U_o = 220$  V (50 Hz) ac, rated capacity  $S = 500$  VA, switching frequency  $f_s = 100$  kHz,  $\Delta u_o \leq 2\%u_o$ ,  $\Delta u_{Cb} \leq 5\%u_{Cb}$ , and  $\Delta i_L \leq 20\%i_L$ . To ensure the operation of the converter, circuit parameters, including  $D$ ,  $C_o$ ,  $C_b$ ,  $L$ , and  $S_1 \sim S'_6$ , are determined.

### A. Designing Duty Cycle $D$

In order to simplify the design of  $D$ ,  $C_o$ , and  $C_b$ , the current  $i_L$  of inductor  $L$  and current  $i_{C_o}$  of filter capacitor  $C_o$  are considered as constant during one switching period  $T_s$ . Key waveforms of the converter during one  $T_s$  are shown in Fig. 5, where  $u_{Cb}$ ,  $i_{Cb}$ , and  $u_{C_o}$  are the voltage across flying capacitor  $C_b$ , the current of  $C_b$ , and the voltage across filter capacitor  $C_o$ , respectively.

During  $t_0 \sim t_2$ ,  $u_{C_o}$  decreases linearly, and then, the decrement  $\Delta u_{C_o-}$  is

$$\Delta u_{C_o-} = \Delta u_o = \int_{t_0}^{t_2} \frac{i_o}{C_o} dt = \frac{i_o}{C_o} (t_2 - t_0) = \frac{i_o}{C_o} \cdot T_s \cdot D. \quad (7)$$

During  $t_2 \sim t_4$ ,  $u_{C_o}$  increases linearly, and the increment  $\Delta u_{C_o+}$  can be derived as

$$\Delta u_{C_o+} = \int_{t_2}^{t_4} \frac{i_{C_o+}}{C_o} dt = \frac{i_{C_o+}}{C_o} \cdot T_s \cdot (1 - D). \quad (8)$$

However,  $\Delta u_{C_o-} = \Delta u_{C_o+}$  in one  $T_s$ , and then,  $i_{C_o+} = Di_o/(1 - D)$ , and  $i_L = i_{C_o+} + i_o = i_o/(1 - D)$ .

During  $t_0 \sim t_1$ ,  $u_{Cb}$  increases linearly, and the increment of  $u_{Cb}$  is given by

$$\Delta u_{Cb+} = \int_{t_0}^{t_1} \frac{i_L}{C_b} dt = \frac{i_o}{C_b(1 - D)} \cdot (t_1 - t_0). \quad (9)$$

During  $t_2 \sim t_3$ ,  $u_{Cb}$  decreases linearly, and the decrement of  $u_{Cb}$  can be obtained

$$\Delta u_{Cb-} = \int_{t_2}^{t_3} \frac{i_L}{C_b} dt = \frac{i_o}{C_b(1 - D)} \cdot (t_3 - t_2). \quad (10)$$

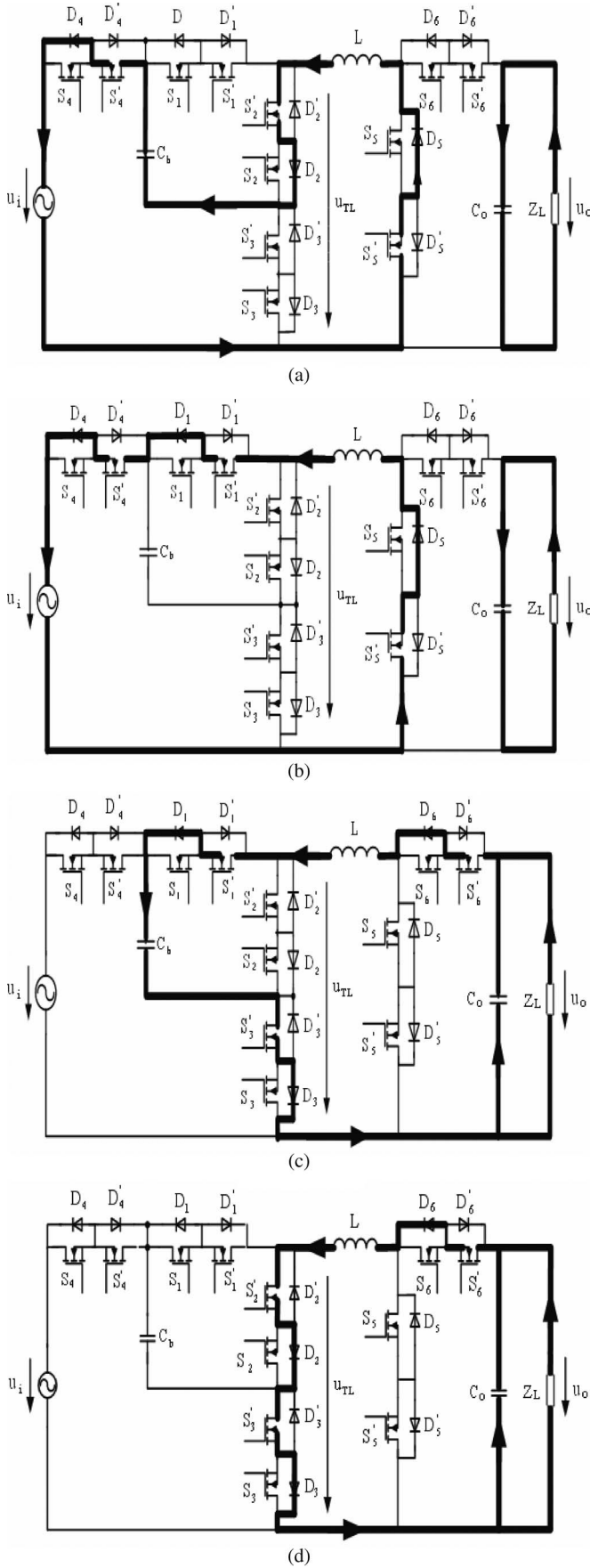


Fig. 4. Topological states during one  $T_s$  in mode B. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

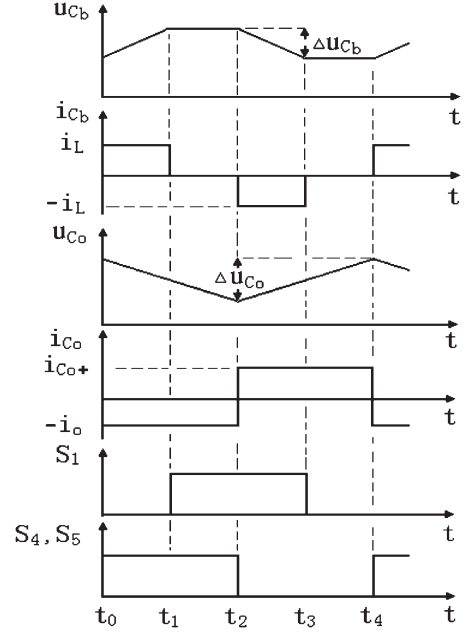


Fig. 5. Key waveforms of buck TL-boost mode cascade TL ac-ac direct converter.

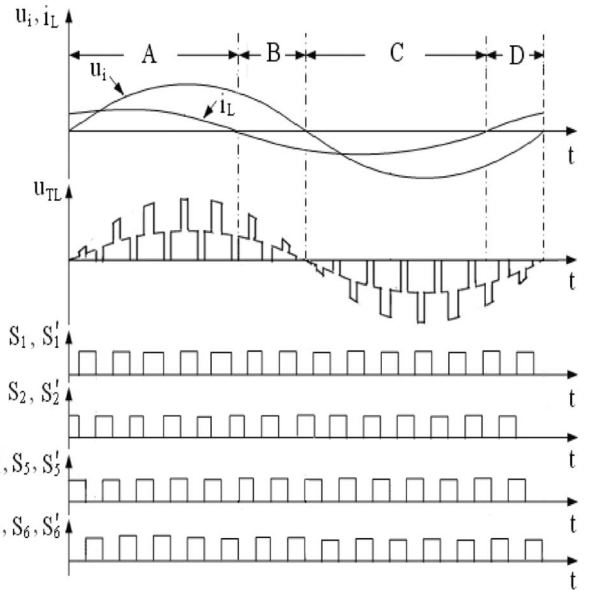


Fig. 6. Principal waveforms of transient output voltage feedback control strategy.

However,  $\Delta u_{Cb+} = \Delta u_{Cb-}$  in one  $T_s$ , and then,  $t_1 - t_0 = t_3 - t_2$ , and  $D' = D$ . From (6),  $U_o/U_i$  can be given by the following:

$$\frac{U_o}{U_i} = \frac{D}{1-D}. \quad (11)$$

Therefore, the maximum and the minimum duty cycles are determined by

$$D_{\max} = 1/(1 + U_{i,\min}/U_o) = 1/(1 + 198/220) = 0.526 \quad (12)$$

$$D_{\min} = 1/(1 + U_{i,\max}/U_o) = 1/(1 + 242/220) = 0.476. \quad (13)$$



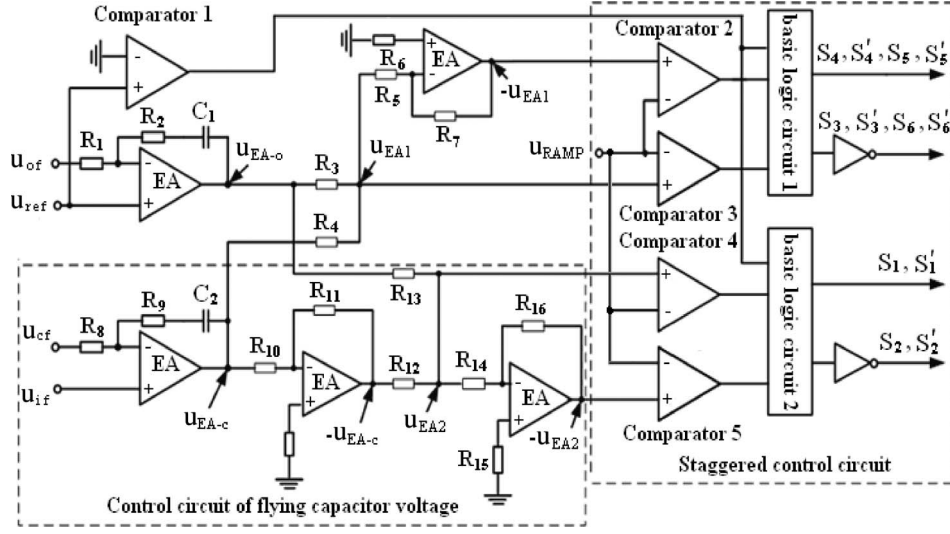


Fig. 7. Control structure block diagram of the presented control strategy.

### B. Designing Filter Capacitor $C_o$

From (7), (12), and  $\Delta u_o \leq 2\%u_o$ ,  $C_o$  must satisfy

$$C_o \geq \frac{I_o \cdot T_s \cdot D_{\max}}{2\%U_o} = \frac{S \cdot T_s \cdot D_{\max}}{0.02U_o^2}$$

$$= \frac{500 \times 10 \times 10^{-6} \times 0.526}{0.02 \times 220^2} = 2.72 (\mu F). \quad (14)$$

The maximum voltage across  $C_o$  is  $\sqrt{2}U_o = \sqrt{2} \times 220 = 311$  (V), so  $C_o$  is chosen as  $4.7 \mu F/630$  V.

### C. Designing Flying Capacitor $C_b$

To simplify the control, let  $(t_1 - t_0)/T_s = 0.25$ . According to (9), (11),  $u_{Cb} = u_i/2$ , and  $\Delta u_{Cb} \leq 5\%u_{Cb}$ ,  $C_b$  must be satisfied with the following expression:

$$C_b \geq \frac{i_o \cdot (t_1 - t_0)}{(1 - D) \cdot 5\% \cdot u_i/2} = \frac{40S \cdot (t_1 - t_0) \cdot D_{\max}}{(1 - D_{\max})^2 \cdot U_o^2}$$

$$= \frac{40 \times 500 \times 10 \times 10^{-6} \times 0.25 \times 0.526}{(1 - 0.526)^2 \times 220^2} = 2.42 (\mu F). \quad (15)$$

The maximum voltage across  $C_b$  is  $\sqrt{2}U_{i,\max}/2 = \sqrt{2} \times 242/2 = 171$  (V), so  $C_b$  is selected as  $4.7 \mu F/630$  V.

### D. Designing Inductor $L$ for Energy Storage

During  $t_0 \sim t_2$ , current  $i_L$  of inductor  $L$  increases. From (11),  $u_{Cb} = u_i/2$ ,  $D = (t_2 - t_0)/T_s$ , and  $(t_1 - t_0)/T_s = 0.25$ , the maximum change of  $i_L$  is

$$\Delta i_L = \frac{u_i - u_{Cb}}{L}(t_1 - t_0) + \frac{u_i}{L}(t_2 - t_1)$$

$$= \frac{(2D - 0.25) \cdot (1 - D)}{2D \cdot L} T_s \cdot u_o. \quad (16)$$

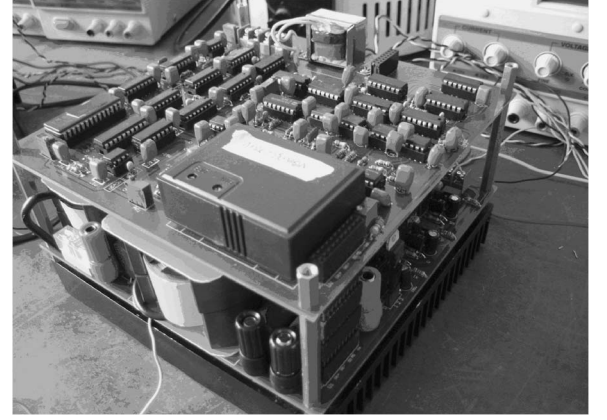


Fig. 8. Prototype of cascade TL ac-ac direct converter.

According to (16),  $\Delta i_L \leq 20\%i_L$ , and  $i_L = i_o/(1 - D)$ ,  $L$  must satisfy

$$L \geq \frac{(2D_{\min} - 0.25) \cdot (1 - D_{\min})^2 \cdot T_s \cdot U_o^2}{0.4D_{\min} \cdot S}$$

$$= \frac{(2 \times 0.476 - 0.25) \times (1 - 0.476)^2 \times 10 \times 10^{-6} \times 220^2}{0.4 \times 0.476 \times 500}$$

$$= 1.186 (\text{mH}). \quad (17)$$

Select  $L = 1.2$  mH.

### E. Determining Power Switches $S_1 \sim S'_6$

The voltage across  $S_1 \sim S'_4$  is obtained as

$$\sqrt{2}U_{i,\max}/2 = \sqrt{2} \times 242/2 = 171(\text{V}). \quad (18)$$

Moreover, the voltage across  $S_5 \sim S'_6$  is

$$\sqrt{2}U_o = \sqrt{2} \times 220 = 311(\text{V}). \quad (19)$$

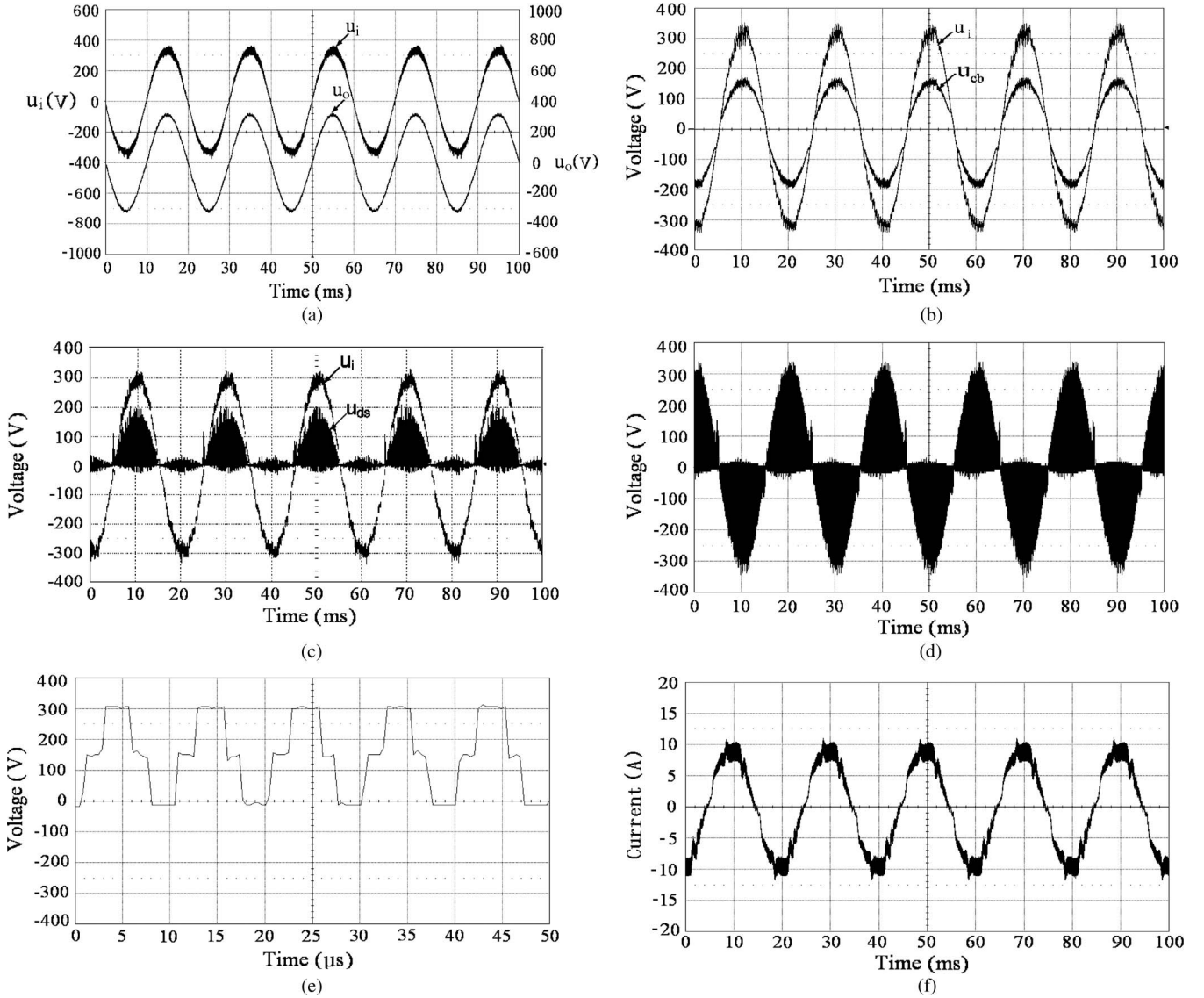


Fig. 9. Experimental waveforms with resistive load ( $R = 96 \Omega$ ). (a) Input voltage  $u_i$  and output voltage  $u_o$ . (b) Voltage across  $C_b u_{Cb}$  and  $u_i$ . (c) Voltage across  $S_1 u_{ds}$  and  $u_i$ . (d) Voltage  $u_{TL}$ . (e) Voltage  $u_{TL}$ . (f) Current  $i_L$  of inductor for energy storage.

The maximum rms current of  $S_1 \sim S'_6$  is given by

$$I_{L,\max} = \frac{I_{o,\max}}{1 - D_{\max}} = \frac{500}{198 \times (1 - 0.526)} = 5.33 \text{ (A)}. \quad (20)$$

Then, MOSFET IRFP460 (500 V/20 A) is chosen for  $S_1 \sim S'_6$ .

## V. MECHANISM FOR CONTROLLING VOLTAGE ACROSS FLYING CAPACITOR

A strategy of the transient output voltage feedback control, shown in Fig. 6, is introduced for the converters. According to the polarity of  $u_i$  and  $i_L$ , the converter will work in four modes: A, B, C, and D.

If voltage  $u_{Cb}$  across flying capacitor  $C_b$  is out of control, TL waveforms of  $u_{TL}$  cannot be achieved. Therefore, a new double transient voltage feedback control strategy of  $u_o$  and  $u_{Cb}$  is presented, whose control structure block diagram is shown in Fig. 7. EA represents the error amplifier. Sample signal  $u_{cf}$  of  $u_{Cb}$  is compared with sample signal  $u_{if}$  of  $u_i$ , and then, error-

amplified signal  $u_{EA-c}$  can be obtained. Meanwhile, sample signal  $u_{of}$  of  $u_o$  is compared with reference voltage  $u_{ref}$ , and then, another error-amplified signal  $u_{EA-o}$  can be got. Voltage  $u_{EA1}$  can be gained by adding  $u_{EA-c}$  to  $u_{EA-o}$ . By comparing  $u_{EA1}$  and  $-u_{EA1}$  with carrier waves  $u_{RAMP}$ , PWM signals  $u_3 \sim u'_6$  can be obtained. Similarly,  $u_{EA2}$  can be gained by adding  $-u_{EA-c}$  to  $u_{EA-o}$ . By comparing  $u_{EA2}$  and  $-u_{EA2}$  with  $u_{RAMP}$ , PWM signals  $u_1 \sim u'_2$  can be got.

In the positive (negative) half cycle of  $u_o$ , once  $u_{Cb} < u_i/2$ ,  $u_{EA-c}$  is positive; then,  $u_{EA1}$  ( $-u_{EA1}$ ) increases, and  $u_{EA2}$  ( $-u_{EA2}$ ) decreases. As the results, the pulses of  $S_4$  and  $S_5$  ( $S'_4$  and  $S'_5$ ) turn wider, and the pulse of  $S_1$  ( $S'_1$ ) turns narrower. The charge time and the discharge time of  $C_b$  turn longer and shorter, respectively, so  $u_{Cb}$  can be controlled to be  $u_i/2$ . On the other hand, if sample signal  $u_{of}$  of  $u_o$  is less than reference voltage  $u_{ref}$ ,  $u_{EA-o}$  is positive, and then,  $u_{EA1}$  and  $u_{EA2}$  ( $-u_{EA1}$  and  $-u_{EA2}$ ) rise. Therefore, the pulses of  $S_1$ ,  $S_4$ , and  $S_5$  ( $S'_1$ ,  $S'_4$ , and  $S'_5$ ) turn wider, so  $u_o$  can be increased to be the expected value.

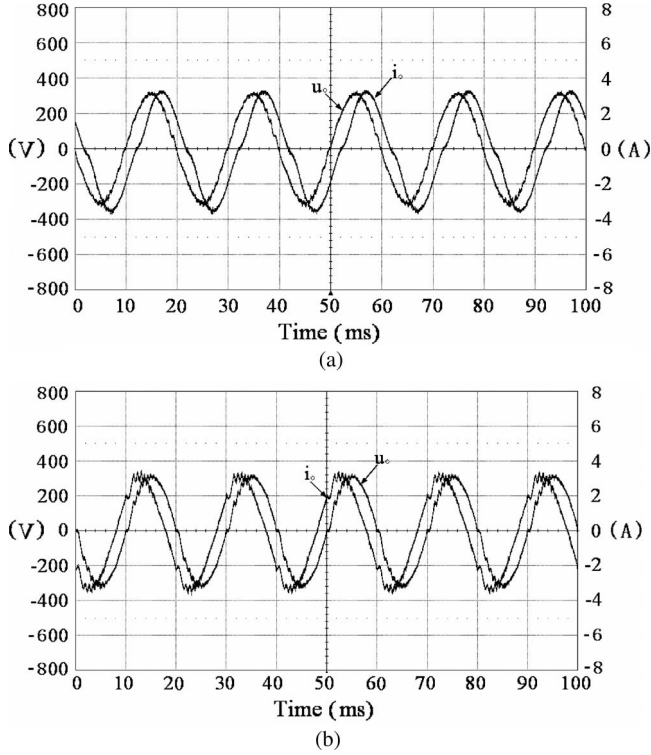


Fig. 10. Experimental waveforms with  $RL$  ( $R = 72 \Omega$ ,  $L = 200$  mH) and  $RC$  load ( $R = 72 \Omega$ ,  $C = 50 \mu\text{F}$ ). (a) Output voltage  $u_o$  and output current  $i_o$ . (b) Output voltage  $u_o$  and output current  $i_o$ .

## VI. PROTOTYPE

The designed and developed prototype is as follows: Buck TL-boost mode circuit topology, double transient voltage feedback control strategy, rated capacity  $S = 500$  VA, input voltage  $U_i = 198\text{--}242$  V (50 Hz) ac, output voltage  $U_o = 220$  V (50 Hz) ac, duty cycle  $D = 0.476 \sim 0.526$ , switching frequency  $f_s = 100$  kHz, inductance for energy storage  $L = 1.2$  mH, flying capacitance  $C_b = 4.7 \mu\text{F}/630$  V, filter capacitance  $C_o = 4.7 \mu\text{F}/630$  V, MOSFET IRFP460 (500 V/20 A) for  $S_1 \sim S'_6$ , and load power factor  $\cos \varphi_L = -0.75 \sim +0.75$ .

The prototype shown in Fig. 8 has the following good performances: rated capacity  $S = 500$  VA, input voltage  $U_i = 198\text{--}242$  V (50 Hz) ac, precision of output voltage  $\leq 1.5$  V, load power factor  $\cos \varphi_L = -0.75 \sim +0.75$ , output voltage THD  $< 3.5\%$ , conversion efficiency at rated power for different types of loads  $\eta \geq 80.7 \sim 85.8\%$ , line power factor at rated different nature load  $\cos \varphi \geq 0.66 \sim 0.94$ , operational time of 120 min at 110% rated load, weight  $< 2.5$  kg, and bulk  $< 175 \text{ mm} \times 170 \text{ mm} \times 130 \text{ mm}$ .

Experimental waveforms of the converter are shown in Figs. 9 and 10. The experimental results have verified that the converter has the following advantages such as low THD of  $u_o$ , symmetrical voltage  $u_{Cb}$  and  $u_{Cb}$  be controlled as  $u_i/2$ , lower voltage across the power switches in the buck TL stage ( $u_i/2$ ), TL ( $u_i, u_i/2, 0$ ) in voltage  $u_{TL}$ , strong adaptability to various loads, etc.

Fig. 11 illustrates how the curves of the line power factor, THD of  $u_o$  and  $u_i$ , and conversion efficiency vary with the load. According to the results, the converter achieves high conversion

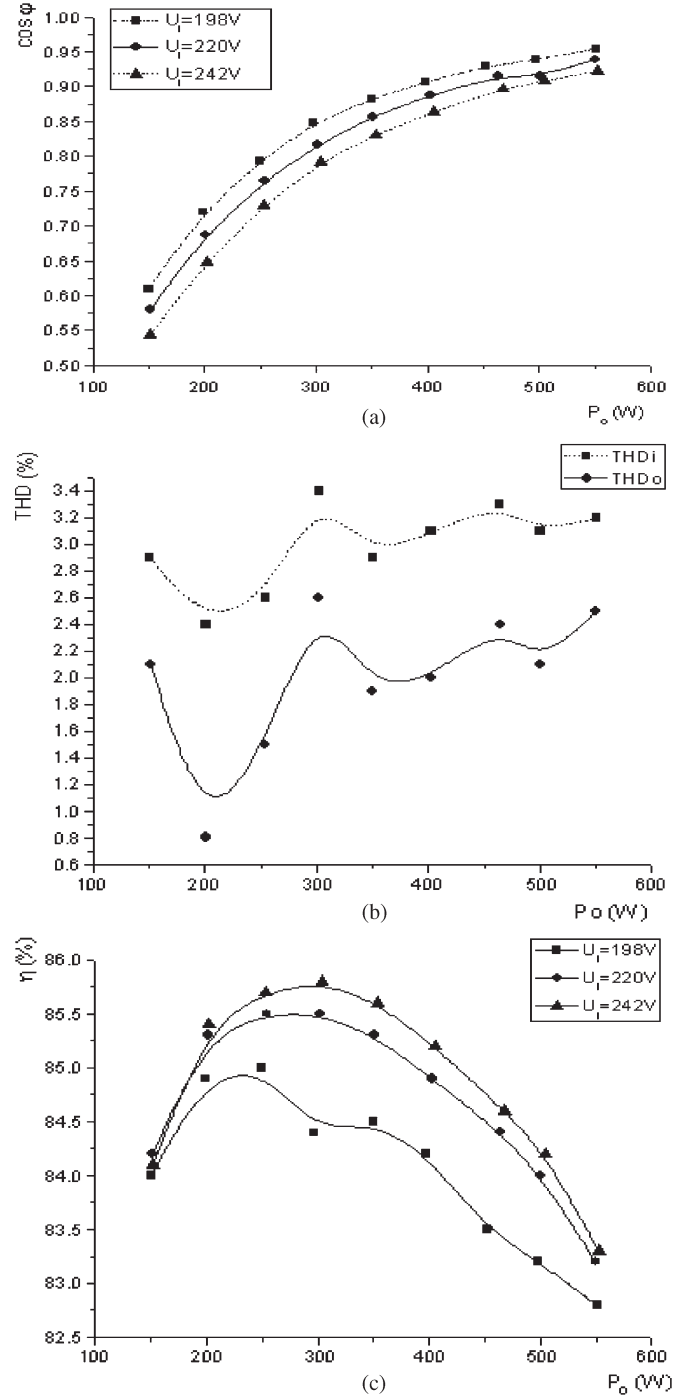


Fig. 11. Line power factor, THD, and conversion efficiency versus the load. (a) Line power factor versus output power. (b) THD of input and output voltages versus output power at  $U_i = 220$  V. (c) Conversion efficiency versus output power.

efficiency, higher line power factor, and low THD of output voltage.

## VII. CONCLUSION

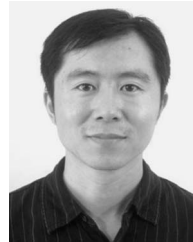
In this paper, a novel family of cascade TL ac-ac direct converters has been proposed based on ac switch cells. The converters directly transfer unsteady high ac voltage with distortion into regulated sinusoidal voltage with low THD. The

topological family includes buck TL–boost, buck–boost TL, and buck TL–boost TL modes. By introducing the double transient voltage feedback control strategy, the TL ac–ac conversion and lower voltage across power switches can be reliably achieved.

This paper also describes the design and the development of a 500-VA 220-V  $\pm 10\%$  50-Hz ac/220-V 50-Hz ac prototype. Experimental results show that the converters reduce the voltage across the power switches in the TL stage to  $u_i/2$ , which is only a half of the traditional two-level ac–ac converters. The input power factor is higher than  $0.66 \sim 0.94$  at rated capacity, which is better than the ac–dc–ac-type TL ac–ac converters. Furthermore, low THD of output voltage and the function of bidirectional power flow are also demonstrated in this paper.

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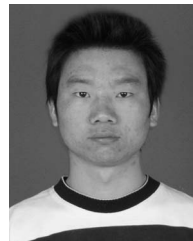
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