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Analog circuit sizing via swarm intelligence

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ABSTRACT

Together with the increase in electronic circuit complexity, the design and optimization processes have to be automated with high accuracy. Predicting and improving the design quality in terms of performance, robustness and cost is the central concern of electronic design automation. Generally, optimization is a very difficult and time consuming task including many conflicting criteria and a wide range of design parameters. Particle swarm optimization (PSO) was introduced as an efficient method for exploring the search space and handling constrained optimization problems. In this work, PSO has been utilized for accommodating required functionalities and performance specifications considering optimal sizing of analog integrated circuits with high optimization ability in short computational time. PSO based design results are verified with SPICE simulations and compared to previous studies.

1. Introduction

Analog integrated circuit (IC) design is a challenging process which involves the characterization of complex tradeoffs between nonlinear objectives and also satisfying required constraints. Those objectives are comprised of design parameters which are ideally accepted as variables and optimum solution set is searched. However, as the circuit complexity increases the search space expands such that obtaining the optimal combination of design parameters by hand becomes a time consuming and unaffordable process. Considering CMOS IC design process, there are several relations that should hold between length, width and width/length ratios of MOS transistors to ensure that the search space is smooth and the optimization process is reliable. Therefore, efficient optimization methods are required for automation of optimal sizing of CMOS analog IC design.

Classical optimization approaches are either deterministic or statistical-based techniques. Deterministic methods, such as Simplex [1], Branch and Bound [2], Goal Programming [3], and Dynamic Programming [4] are effective only for small size problems. These optimization techniques impose several limitations for multi-criteria constrained problems due to their inherent solution mechanisms and their tight dependence on the algorithm parameters. Most of the optimization problems require different types of variables, objective and constraint functions simultaneously in their formulation. Statistical methods generally start with finding a "good" DC quiescent point, which is provided by the

skilled analogue designer. Following, a simulation-based tuning procedure takes place. However these statistic-based approaches are time consuming and do not guarantee the convergence towards the global optimum solution [5]. Therefore, classic optimization procedures are generally not adequate for optimal sizing of analog integrated circuits.

Heuristics are necessary to solve big size problems and/or with many criteria [6]. They can be adapted to suit specific problem requirements. Even though they do not guarantee to find in an exact way the optimal solution, they provide good approximation of it within an acceptable computing time [7]. Some mathematical heuristics that were previously utilized were Local Search [8], Simulated Annealing (SA) [9,10], Tabu Search (TS) [11,12], Genetic Algorithms (GA) [13,14], etc.

However, efficiency of these techniques is highly dependent on the algorithm parameters, the dimension of the solution space and the number of variables. Actually, most of the circuit design optimization problems simultaneously require different types of variables, objective and constraint functions in their formulation. Hence, the abovementioned optimization procedures generally require long computation time when complexity of the problem increases. In order to overcome these drawbacks, a new set of nature inspired heuristic optimization algorithms were proposed. The thought process behind these algorithms is inspired from the collective behavior of decentralized, self-organized systems. It is known as Swarm Intelligence (SI) [15]. SI systems typically employ a population of simple agents interacting locally with each other and with their environment. These particles obey to very simple rules, and although there is no centralized control structure dictating how each particle should behave. Local interactions between them lead to the emergence of complex global behavior. Most famous such SI techniques are Ant Colony Optimization (ACO) [16],

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Artificial Bee Colony (ABC) optimization [17] and Particle Swarm Optimization (PSO) [18,19]. PSO has been in existence for almost a decade, which is a relatively short period when compared to some of the well known evolutionary computation paradigms and has been shown to offer good performance in various application domains [20].

Above mentioned optimization methods are incorporated into analog computer-aided design (CAD) tools for optimal sizing of complex ICs together with topology selection [21] and actual circuit layout [22]. Historically, researchers developed two mainstreams of analog automation methodologies. One of the early approaches uses optimization-based method which optimizes a set of performance constraints characterized by complicated tradeoffs and makes repetitive use of detailed circuit simulator embedded in the inner loop of optimization engine. These techniques require many iterations to adjust transistor sizes and optimization engine needs to evaluate corresponding performance at each cycle. Second approach is equation-based method which is based on inverse process of circuit analysis technique. Since sizing of a circuit is done mathematically, the automation is much faster while accuracy is not as good as the first approach due to the simplified device equations and approximations [23,24]. Comparison of previously proposed analog CAD tools is given in Table 1 [22–31]. Among the CAD tools tabulated in Table 1, DELIGHT.SPICE, STAIC and OPASYN utilize classical optimization techniques while IDAC, MAELSTROM, ASTRX/OBLX, ASLIC, and OASYS are heuristic based systems. Kruiskamp and Leenaerts [32] developed a GA based CMOS operational amplifier synthesizer (DARWIN) for topology selection and circuit sizing. In [33], sizing rules method is proposed for CMOS and bipolar analog IC synthesis. Sripramong and Toumazou [34] introduced an automated circuit design system for the evolution and subsequent invention of CMOS amplifiers. This system utilized genetic programming for evolving new circuit topologies and current-flow analysis for screening and correcting circuits. In [35], it was proved that CMOS op-amp design can be approximated as convex optimization problem that can be solved using geometric programming techniques. In [36], an evolution-based methodology named memetic single-objective evolutionary algorithm is developed for automated sizing of high-performance analog IC circuits. Guerra-Gomez et al. [37] proposed multi-objective evolutionary algorithm based on decomposition (MOEA/D) for optimization of second generation current conveyors (CCII). Mentioned system uses HSPICE as circuit evaluator. Considering optimal CCII design without any circuit evaluator; a multi-objective heuristic [38,39] and PSO algorithm [40–42] are utilized by formulating the requirements for the design of CCII in terms of boundaries on performance functions. Tawdross and König [43] investigated PSO as an alternative to GA for field programmable analog scalable device array reconfiguration. For this purpose an operational amplifier with particular design constraints was designed using PSO taking into different external influences such as high temperature and fabrication faults. Having successful results authors extended their PSO based dynamic hardware design

environment to functional block level [44]. A 3-bit ADC structure is developed using previously designed op-amps and resistors. In [45], PSO algorithm is extended to a hierarchical scheme for automatic sizing of low power analog circuits where simulation of circuits is performed with Cadence Spectre. Tulunay and Balkir [46] proposed an automatic synthesis tool of a cascade low noise amplifier (LNA). In [42], PSO technique is utilized for optimal sizing of CMOS LNA with inductive degeneration design. Choi and Allstot [47] developed a SA based synthesis tool that includes an adaptive tunneling mechanism and post-optimization sensitivity analysis with respect to design, process and temperature variations. A detailed investigation about the state of the art in applying EAs for the synthesis and sizing of analog ICs is presented in [48].

This main objective of this study is to explore Particle Swarm Optimization algorithm on analog circuit design automation. PSO-based method is applied to two analog integrated circuit design problems with particular technology parameters. The problem considered in this work is the optimal CMOS transistor sizing for minimum area oriented optimization, which is only a part of a complete analog circuit CAD tool. Other parts which are beyond the scope of this work are the topology selection and actual circuit layout. The optimal transistor sizing of the CAD process remains between these two tasks. As reported in the literature, simulation-based optimization technique requires very long execution time and equation-based methods are less accurate than the former method. Therefore, optimization methods with high accuracy and short computation time are necessary for analog circuit design automation. PSO as a global optimization method has fewer primitive mathematical operators than in GA (e.g. reproduction, mutation and crossover) and those mathematical operations require more fine-tuning of own parameters which leads to longer computation time as explained in Section 2. Section 3 describes analog integrated circuit structures and states design specifications used in optimal sizing task. PSO-based method for integrated circuit design is investigated in Section 4. Following, Section 5 provides simulation results of the proposed method, comparable to previous methods, which are validated with SPICE simulator. Finally, Section 6 concludes with a discussion of PSO based design results and suggests possible extensions.

2. Particle swarm optimization

Particle swarm optimization (PSO) is an evolutionary computation method based on the social behavior, movement and intelligence of swarms searching for an optimal location in a multidimensional search area [18]. The approach uses the concept of population and a measure of performance similar to the fitness value used with evolutionary algorithms. Population consists of potential solutions called particles. Each particle is initialized with a random position value. In each iteration of simulation, the fitness function is evaluated by taking the current position of the particle in the solution space and two best values (p_{best}, g_{best}). Personal best value, p_{best}, is the location of the best fitness value obtained

Table 1
The error rate and synthesis time of various analog CAD tools [23,24].

Tool	Synthesis method	Error	Synthesis time
IDAC [25]	Equation-based	15%	Few seconds
OASYS [26]	Equation-based	25%	Few seconds
ISAID [27]	Equation-based + post optimization	14%	Not reported
STAIC [22]	Equation-based	24%	3 min
DELIGHT.SPICE [28]	Optimization-based (circuit simulator)	0%	18 h
MEALSTROM [29]	Optimization-based (circuit simulator)	0%	3.6 h
ASTRX/OBLX [30]	Optimization-based (AWE + equations)	30%	11.8 h
OPASYN [31]	Optimization-based (equations)	20%	1 min
ASLIC [24]	Equation-based	15–20%	Few seconds

For *each* particle
 Load its initial random vector;

For each particle
 Assign its initial vector as its pbest vector;

While maximum iteration is not attained
{
 Assign the first particle's pbest to gbest;
   For each particle except the first one {
     If its pbest satisfies all the constraints {
       If its pbest value fits to cost function better than the gbest {
         Assign its pbest as gbest;
                                                                }
                                                            }
                                                        }

 For each particle {
   Calculate particle velocity according to (1);
   Update particle position according to (2);
                                            }
     For each particle {
       If the particle's current value and its pbest value both satisfy the
constraints {
         If the particle's current value fits the function better than its pbest value
{
           Assign its current value as its pbest value;
                                                    }
                                                }
       Else if the particle's current value and its pbest value both don't satisfy
the constraints {
         If the particle's current value fits the function better than its pbest value
{
           Assign its current value as its pbest value;
                                                    }
                                                }
         Else if only the particle's current value satisfies the constraints
{
           Assign its current value as its pbest value;
                                                            }
                                        }
 }

Fig. 1. Procedures of PSO algorithm.

so far by the particle. Global best value, g_{best}, is the location of the best fitness value achieved so far considering all the particles in the swarm [18,19].

In particle population matrix, containing N number of particles, ith particle with a feature number of D is denoted as $x_i = [x_{i1}, x_{i2}, ..., x_{iD}]$. For each iteration, the velocity and the position vector of the ith particle in NxD dimension of the search space are updated as follows [18]:

$$v_{id}^{k+1} = w.v_{id}^k + c_1.rand_1^k.(pbest_{id}^k - x_{id}^k) + c_2.rand_2^k.(gbest_d^k - x_{id}^k) \quad (1)$$

$$x_{id}^{k+1} = x_{id}^k + v_{id}^{k+1} \quad (2)$$

Here, the range of i, d and k indices are defined as $\{1...N\}$, $\{1...D\}$ and $\{1...max\_iteration\_number\}$ respectively. The acceleration factors c_1 and c_2 indicate the relative attraction toward p_{best} and g_{best} respectively. Following $rand_1$ and $rand_2$ are random numbers uniformly distributed between zero and one. Inertia weight parameter w controls the tradeoff between the global and the local search capabilities of the swarm. Initially w should be chosen less than one and should be decreased linearly in each iteration.

Generally PSO has the advantage of being very simple in concept, easy to implement and computationally efficient algorithm. Since updates in algorithm consist of simple adding and multiplication operators and no derivation operation is included, computation time is dramatically decreased compared to other heuristic algorithms [49,50]. In order to avoid premature convergence, PSO utilizes a distinctive feature of controlling a balance between global and local exploration of the search space which prevents from being stacked to local minimum [18,19]. Procedures of PSO algorithm is given in Fig. 1.

3. Analog integrated circuit structures

Analog IC design in general is perceived as less systematic and more heuristic and knowledge-intensive in nature than digital IC design. The variety of circuit schematics and the number of conflicting requirements and corresponding diversity of device sizes are also much larger. In addition analog circuits are more sensitive to nonidealities and all kinds of higher order effects and parasitic disturbances [23].

The problem considered here is the optimal selection of transistor dimensions, which is only a part of a complete analog circuit CAD tool. Actually, analog sizing is a constructive procedure that aims at mapping the circuit specifications (objectives and constraints on performances) into the design parameter values [39]. In other words, the performance metrics of the circuit, such as gain, power dissipation, occupied area, etc. have to be formulated in terms of the design parameters [51]. Then, these design parameters such as device sizes and bias currents should be adjusted under multiple design objectives and constraints. The many degrees of
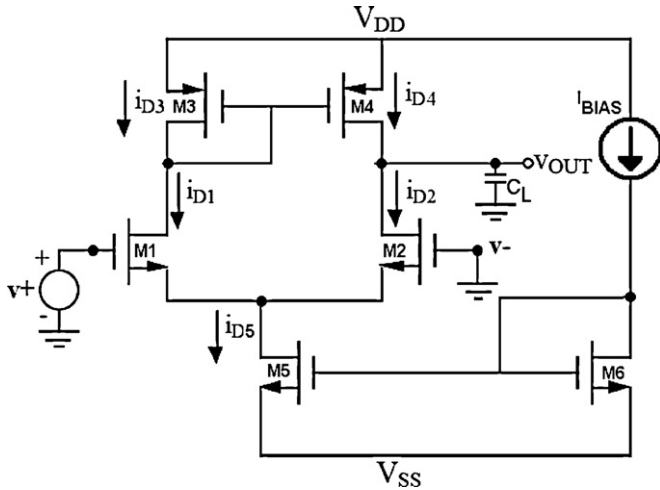
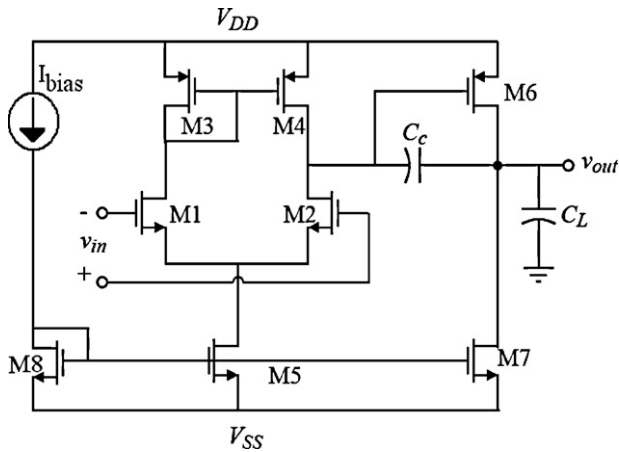**Fig. 2.** Differential amplifier with current mirror load [52].

Fig. 3. Two stage operational amplifier [52].

freedom in parameter space as well as the need for repeated circuit performance evaluation made this a lengthy and tedious process [31]. Here, particular specifications for specified topologies of a differential amplifier and an operational amplifier (op-amp) are aimed to be met by adjusting design parameters such as device sizes and bias currents with PSO algorithm, while minimizing the total MOS transistor area. The configurations considered in this study are a differential amplifier with a current mirror load (Fig. 2) and a two stage CMOS op-amp (Fig. 3). Both can be characterized by a number of specifications as given below. More detailed description can be found in [24,35,50,52]:

- Common mode rejection ratio (CMRR)
- Input offset voltage (V_{OS})
- Slew rate (SR)
- Power dissipation (P_{diss})
- Small signal characteristics ($A_v, \omega_{-3dB}, f_t, f_{-3dB}$)
- Phase margin
- Input common mode range (ICMR)
- Power supply rejection ratio (PSRR)

Small-signal differential voltage gain (A_v), cut-off frequency (f_{-3dB}), unity gain bandwidth (f_t), maximum and minimum input common mode range voltages ($V_{IC(max)}, V_{IC(min)}$), slew rate (SR) and power dissipation (P_{diss}) as design specifications and output capacitance (C_L), compensation capacitance (C_c) and MOS transistor

dimensions as design parameters are provided within limits. Equations defining each specification [35,50,52] are utilized for cost function of PSO based analog IC design and are considered for obtaining MOS device sizes (as in Figs. 2 and 3) and moreover minimizing the total MOS transistor area.

A. *Constraints and objectives for differential amplifier*
- Determination of the range of I_{d5} (I_{ss}) to satisfy both SR and P_{diss}.
- Design of W_1/L_1 (W_2/L_2) to satisfy A_v
- Design of W_3/L_3 (W_4/L_4) to satisfy the upper ICMR
- Design of W_5/L_5 (W_6/L_6) to satisfy the lower ICMR

B. *Constraints and objectives for operational amplifier*
- Selection of minimum value for C_c.
- Determination of I_{d5} (I_{ss}) to satisfy SR
- Design of W_1/L_1 (W_2/L_2) using the transconductance of the differential input stage
- Design of W_3/L_3 (W_4/L_4) to satisfy the upper ICMR
- Design of W_5/L_5 (W_8/L_8) to satisfy the lower ICMR
- Design of W_6/L_6 assuming balanced conditions

$$\frac{W_6}{L_6} = \frac{W_4}{L_4}\frac{g_{m6}}{g_{m4}} \tag{3}$$

where

$$g_{m6} \geq 10g_{m1} \tag{4}$$

and

$$g_{m1} = 2\pi f_t C_c \tag{5}$$

assuming zero z_1 is placed beyond ten times f_t [52]

$$g_{m4} = \sqrt{2K'_4\left(\frac{W_4}{L_4}\right)I_{d4}} \tag{6}$$

- Calculation of I_{d6} which will most likely determine the majority of the power dissipation.

$$I_{d6} = \frac{g_{m6}^2}{2K'_6(W_6/L_6)} \tag{7}$$

- Design of W_7/L_7 to achieve the desired current ratios between I_{d5} and I_{d6}

$$\frac{W_7}{L_7} = \left(\frac{W_5}{L_5}\right)\frac{I_6}{I_5} \tag{8}$$

4. PSO based analog integrated circuit design

In order to investigate the usage of PSO in analog IC design, optimal design of two basic analog circuit structures are carried out. The aim of both cases is to minimize total MOS transistor area while satisfying design specifications and design parameter constraints. In each case study, by establishing design parameters and specifications to PSO, the optimal circuit structure is aimed to be designed by the algorithm. Design problem has been introduced to PSO by composing an equation consists of input variables and design parameters as a cost function (CF).

In the beginning of the algorithm, a certain range is determined for both design specifications and design parameters by human designer. Input variables are also determined by the designer and dependent to preferential technology parameters. PSO should minimize CF and obtain design criteria and design parameter values for the given range which provides minimum CF value (Fig. 4).
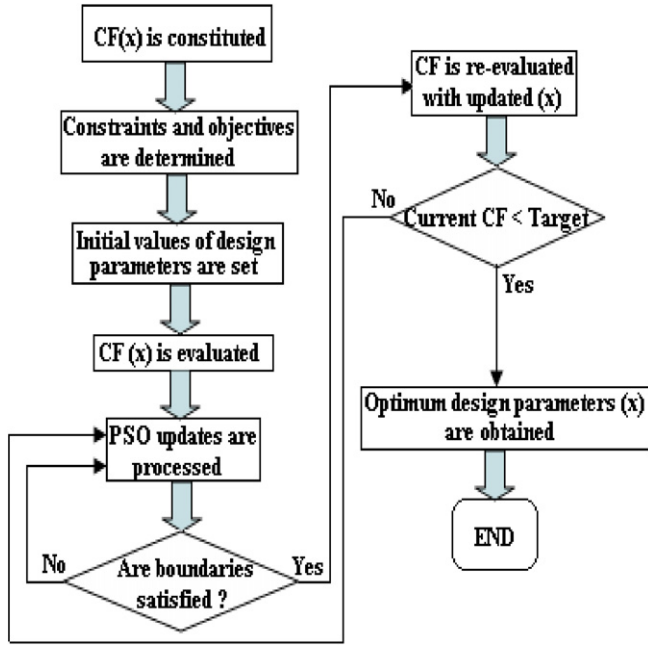
Fig. 4. Flowchart of PSO based IC design methodology.

The starting point of design consists of two types of information. First type of information such as the technology and the power supply is set by the designer. The other type of information is the design criteria. The range of each criteria and design parameter, power supply values and technology information are set as inputs to PSO based design scheme (Table 2) and PSO algorithm should obtain the solution set that consists the exact values of design parameters (C_L, C_c and $(W/L)_k$ where $k = 1.6$ for differential amplifier and $k = 1.8$ for operational amplifier) and design specifications ($V_{IC(max)}$, $V_{IC(min)}$, SR, P_{diss}, A_v, f_{-3dB}, f_t) for given ranges.

The design scheme is implemented with the relationships that describe design specifications to solve for DC currents and W/L values of all MOS transistors. Simulations are carried out using TSMC 0.35 μm model parameters.

PSO algorithm is constructed using MATLAB R2008a. Initial population matrix size was 10×7 where row number of 10 indicates the number of particles in the population and column number of 7 is the dimension of particle vector. Particle vector structure for each analog circuit structure is expressed in (9) and (10).

$$X_{difamp} = [SR, C_L, A_v, f_{-3dB}, V_{IC\,min}, V_{IC\,max}, P_{diss}] \qquad (9)$$

$$X_{opamp} = [SR, C_L, A_v, f_t, V_{IC\,min}, V_{IC\,max}, P_{diss}] \qquad (10)$$

where SR is the slew rate (V/μm), C_L is the output capacitance (pF), A_v is the gain (V/V), f_{-3dB} is the cut-off frequency (KHz), f_t is the unity gain bandwidth (MHz), P_{diss} is the power dissipation (μW),

Table 2
Inputs and outputs for PSO based design scheme.

Components in CF	Information	Input/output for PSO
V_{DD}, V_{SS} V_{TN}, V_{TP} $\mu_n C_{ox}$, $\mu_p C_{ox}$	• Set by human designer • Fabrication technology dependent	Input
C_L, C_c $(W/L)_k$ f_{-3dB}, f_t $V_{IC(max)}$, $V_{IC(min)}$ SR P_{diss} A_v	• Exact results for the given ranges	Output

Table 3
Design parameters obtained with Darwin and PSO.

Differential amplifier with current mirror load design parameters	Darwin [32]	PSO
I_{bias} (μA)	2	125
W_1/L_1, W_2/L_2 (μm/μm)	240/13.2	29.4/3.5
W_3/L_3, W_4/L_4 (μm/μm)	7.3/7.7	11.3/3.5
W_5/L_5 (μm/μm)	4.6/2.4	4.2/1.4
W_6/L_6 (μm/μm)	2.4/2.4	4.2/1.4
C_L (pF)	2	5

$V_{IC(min)}$ (V) and $V_{IC(max)}$ (V) are the lower and upper limits of ICMR, respectively.

Velocity update parameters c_1, c_2 and w were selected as 1.7, 1.7 and 0.99, respectively. The algorithm runs for upper limit of 100 iterations. CF is defined as the total area that MOS transistors occupy and given in (11).

$$CF = \sum_{k=1}^{T} (W_{(k)} \times L_{(k)}) \qquad (11)$$

where T is the total number of MOS transistors of the designed circuit. The target value of CF is aimed to be smaller than 300 μm^2 for both design cases.

5. Simulation results

This section provides the simulation results of PSO based IC design methodology with respect to previous methods.

5.1. Simulation results for differential amplifier

PSO is utilized for a differential amplifier with current mirror load having design specifications of SR ≥ 10 V/μs, A_v > 100 V/V, f_{-3dB} ≥ 100 kHz, −1.5 V ≤ ICMR ≤ 2 V, P_{diss} ≤ 1 mW with inputs of V_{DD} = −V_{SS} = 2.5 V, V_{TN} = 0.4761 V, V_{TP} = −0.6513 V, K'_n = 181.2 μA/V^2, K'_p = 65.8 μA/V^2. Constraints for design parameters are set as C_L > = 5 pF, 100 ≥ $(W/L)_k$ ≥ 3. In order to minimize the channel modulation effect, MOSFET length values are chosen as $L_1 = L_2 = L_3 = L_4 = 3.5$ μm and $L_5 = L_6 = 1.4$ μm.

Target value of CF is aimed to be smaller than 300 μm^2. A total MOS transistor area of 296 μm^2 with each MOSFET width (W_n, W_p), I_{bias} and C_L is obtained within 582 epochs in 25.02 s with Intel Core2 CPU T5500 @1.66 GHz.

Differential amplifier with current mirror load is redesigned using the resulting design parameters in SPICE simulator to validate that PSO based design is satisfying desired specifications. SPICE simulations (Figs. 5–8) demonstrate that PSO based design not only satisfies all specifications and design constraints but also minimizes total MOS area with respect to DARWIN synthesizer [32] as given in Tables 3 and 4.

5.2. Simulation results for operational amplifier

Considering two stage operational amplifier, PSO is utilized for design specifications of SR ≥ 10 V/μs, f_t ≥ 3 MHz, A_v > 1000 V/V, −1.5 V ≤ ICMR ≤ 2 V, P_{diss} ≤ 2.5 mW with PSO inputs as same with previous design scheme. Constraints for design parameters are set as C_L > = 10 pF, 100 ≥ $(W/L)_k$ ≥ 2. In order to minimize the channel modulation effect, all MOSFET length values are chosen as 2 μm [53].

Target value of CF is aimed to be smaller than 300 μm^2. PSO based design method resulted in a total MOS transistor area of 265.8373 μm^2 along with exact values of design specification
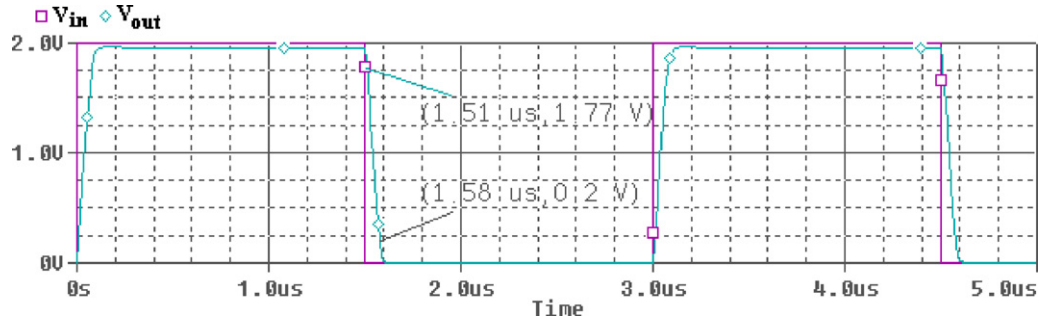
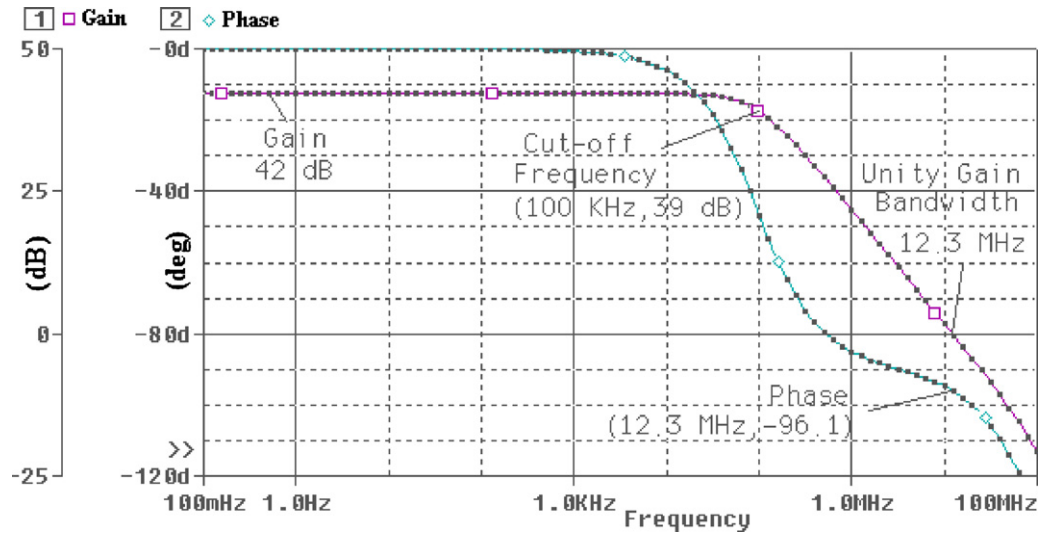**Fig. 5.** Slew rate of PSO based differential amplifier with current mirror load.

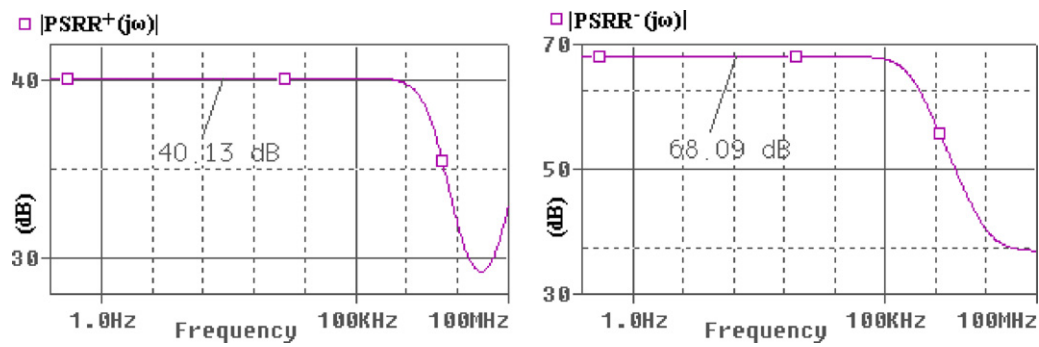**Fig. 6.** Gain and phase margin of PSO based differential amplifier with current mirror load.

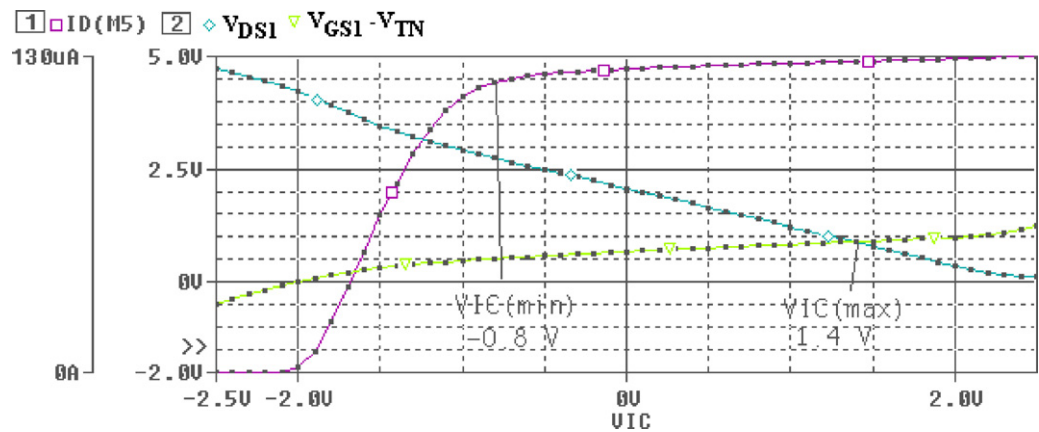**Fig. 7.** PSRR of PSO based differential amplifier with current mirror load.

Fig. 8. ICMR of PSO based differential amplifier with current mirror load.

Table 4
Comparison of Darwin and PSO by means of design specifications.

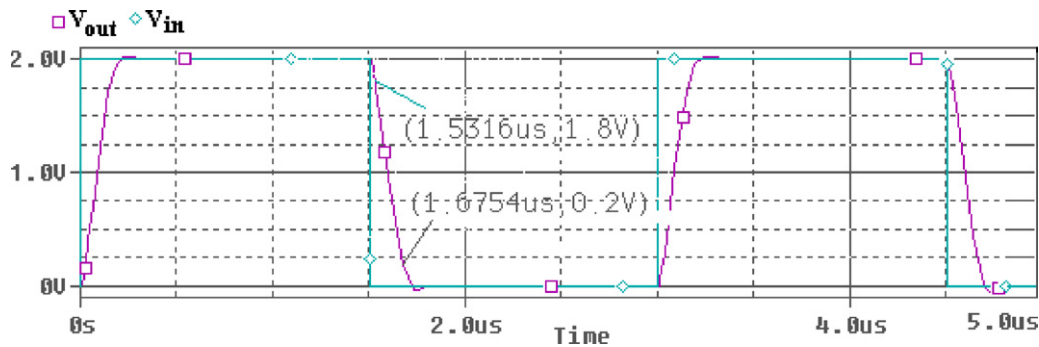| Differential amplifier with current mirror load – design criteria	Specifications	Darwin [32]	PSO (SPICE simulator)
Output capacitance (pF)	≥5	2	5
Slew rate (V/μs)	≥10	3.2	22.4
Power dissipation (μW)	≤2000	31	1260
Phase margin (°)	>45	72	83.8
Cut-off frequency (kHz)	≥100	–	100
Gain (dB)	>40	60	42
$V_{IC(min)}$ (V)	≥−1.5	−1.3	−0.8
$V_{IC(max)}$ (V)	≤2	1.9	1.4
CMRR (dB)	>40	–	84.2
PSRR$^+$ (dB)	>40	–	40.1
PSRR$^-$ (dB)	>40	–	68
V_{os} (mV)	<50	–	45.91
Total area (m^2)	$<3 \times 10^{-10}$	65×10^{-10}	2.96×10^{-10}

Fig. 9. Slew rate of PSO based two-stage operational amplifier.

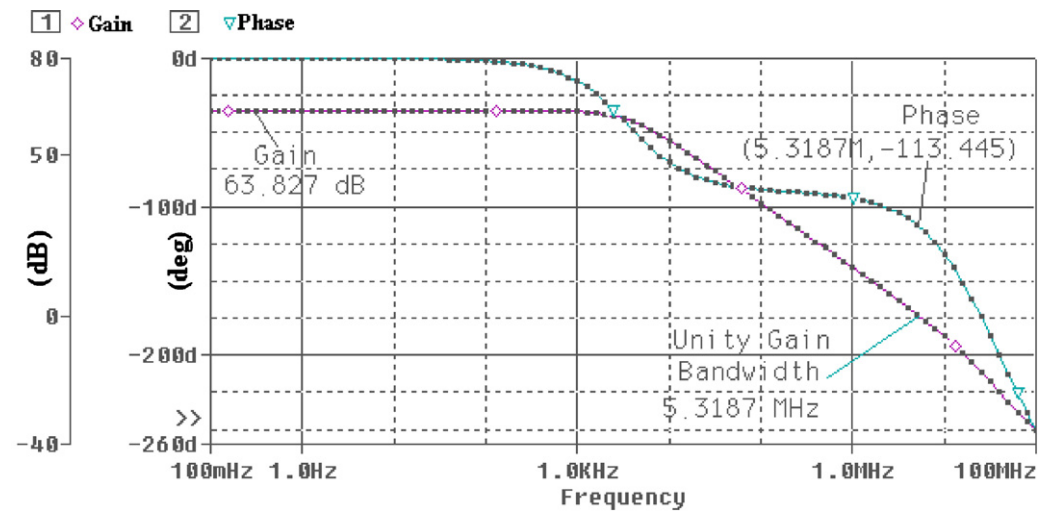**Fig. 10.** Gain and phase margin of PSO based two-stage operational amplifier.

and design parameters (W_n, W_p, I_{bias}, C_c, C_L). Design process concluded after 100 epochs with a total execution time of 8.6 s with Intel Core2 CPU, T5500 @1.66 GHz [53]. Two-stage operational amplifier is redesigned using the resulting design parameters in SPICE simulator in order to validate PSO based design is satisfying the specifications. SPICE simulations (Figs. 9–12) demonstrate that PSO based design not only satisfies all specifications and design constraints but also minimizes total MOS area with respect to convex optimization method [35] as given in Tables 5 and 6.

Table 5
Design parameters obtained with Convex opt. and PSO.

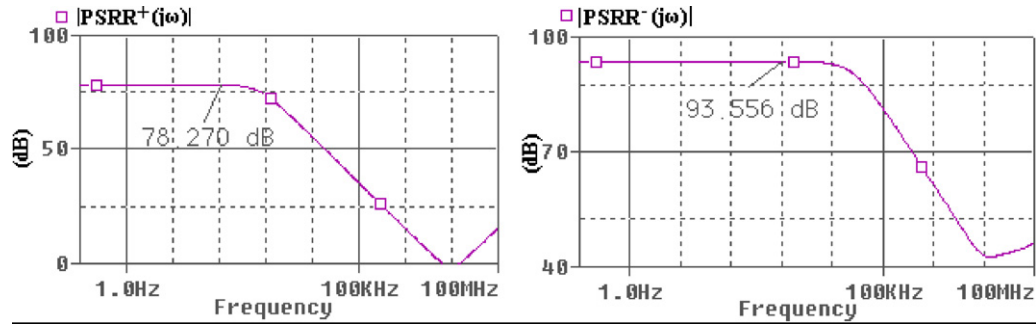| Two-stage op-amp design parameters	Convex opt. [35]	PSO [53]
I_{bias} (μA)	10	40.39
$W_1/L_1, W_2/L_2$ (μm/μm)	232.8/0.8	4.9/2
$W_3/L_3, W_4/L_4$ (μm/μm)	143.6/0.8	5.9/2
W_5/L_5 (μm/μm)	64.6/0.8	2.1/2
W_6/L_6 (μm/μm)	588.8/0.8	90.9/2
W_7/L_7 (μm/μm)	132.6/0.8	16.3/2
W_8/L_8 (μm/μm)	2/0.8	2.1/2
C_L (pF)	3	10
C_c (pF)	3.5	3

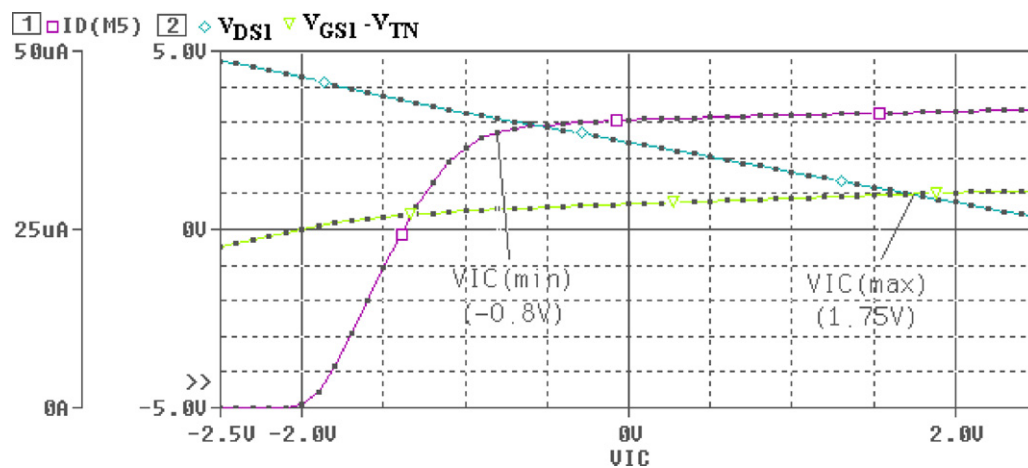Fig. 11. PSRR of PSO based two-stage operational amplifier.

Fig. 12. ICMR of PSO based two-stage operational amplifier.

Table 6
Comparison of convex optimization and PSO by means of design specifications.

Two-stage operational amplifier design criteria	Specifications	Convex optimization [35]	PSO (SPICE simulator) [53]
Output capacitance (pF)	≥10	3	10
Slew rate (V/μs)	≥10	88	11.13
Power dissipation (μW)	≤2500	5000	2370
Phase margin (°)	>45	60	66.55
Unity gain bandwidth (MHz)	≥3	86	5.32
Gain (dB)	>60	89.2	63.8
$V_{IC(min)}$ (V)	≥−1.5	–	−0.8
$V_{IC(max)}$ (V)	≤2	–	1.75
CMRR (dB)	>60	92.5	83.74
PSRR+ (dB)	>70	116	78.27
PSRR− (dB)	>70	98.4	93.56
Total area (m²)	<3 × 10⁻¹⁰	82 × 10⁻¹⁰	2.65 × 10⁻¹⁰

6. Conclusion

Analog IC design mainly consists of topology choice, sizing task and the generation of layout. The problem considered here is the optimal selection of transistor dimensions, which is only a part of a complete analog circuit CAD tool. Actually, analog sizing is a constructive procedure that aims at mapping the circuit specifications where the performance metrics of the circuit, such as gain, power dissipation, occupied area, etc. have to be formulated in terms of the design parameters. Following, these design parameters such as device sizes and bias currents should be adjusted under multiple design objectives and constraints. The many degrees of freedom in parameter space as well as the need for repeated circuit performance evaluation made this a lengthy and tedious process. Here, particular specifications for specified topologies of a differential amplifier with current mirror load and a two-stage operational amplifier are aimed to be met by adjusting design parameters such as device sizes and bias currents with PSO algorithm.

Design equations of each analog circuit are utilized for cost function of PSO algorithm, since numerous design specs are of concern. Considering differential amplifier with current mirror load, PSO-based design method is utilized for TSMC 0.35 μm technology parameters and design process is concluded in 25 s. PSO-based design for two-stage amplifier is concluded in 8.6 s after 100 iterations. Resulting design parameters for each analog circuit are utilized for redesign in SPICE simulator in order to validate the exact values of design specifications obtained with PSO. Consequently, PSO based design scheme satisfied all the design specifications and minimized total design area with respect to former methods. Considering both design cases, PSO proved its efficiency on analog IC design with high optimization ability in short computation time. As a further work, performance of other EA techniques could be

investigated by means of accuracy and computational time by utilizing EKV modeling in analog IC sizing issues.

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