A Single Switch Buck-Boost Converter with a High Conversion Ratio

David M. Van de Sype*, Koen De Gussemé, Wouter R. Ryckaert,
Alex P. Van den Bossche, and Jan A. Melkebeek
Electrical Energy Laboratory (EELAB)
Department of Electrical Energy, Systems and Automation (EESA)
Ghent University
Sint-Pietersnieuwstraat 41
B-9000 Gent, Belgium
*Tel.: +32 9 2647914, Fax: +32 9 2643582
*e-mail: David.VandeSype@UGent.be
http://eesa.UGent.be

Acknowledgement

Keywords

Converter circuit, soft switching

Abstract

To supply a high voltage load from a low voltage source (e.g. battery pack) often a converter is required with a high conversion ratio. Boost converter topologies with coupled inductors have emerged displaying a high efficiency, a low overall component count, a simple topology, and the need for only a single low-voltage active switch. However, in some applications the output of the converter must be capable of reaching voltages below the input voltage. To solve this problem, a buck-boost-converter topology can be derived from the boost converter with coupled inductors. However, if the different positions for the capacitors in the buck-boost topology are considered, several variants can be distinguished. The properties of the different topological variations are studied. Eventually, a topological choice is made based on the proposed criteria for a 175-V supply, converting 175 W from a 24-V battery. The theoretical results are compared to the results retrieved from a prototype converter.

I. Introduction

Nowadays, a lot of applications that were formerly supplied from the mains, have become battery operated (e.g. electric drilling machines, other electric hand equipment, electric kitchenware, electric lawn mowers, etc.). In most of these applications low-voltage motors are applied that in many cases have a low efficiency (low-voltage commutator motors), suffer from a low power-weight ratio or are very expensive. Nevertheless, the universal series motor, the motor used in most mains operated equipment, is rather efficient ($\eta \approx 70\%$), has a high power-weight ratio (0.5 kW/kg) and is very cheap [1]. Moreover, this motor can also be supplied directly from a

dc source. The main disadvantages of the universal series motor are the limited lifetime, the required maintenance and, for battery equipment, the high supply voltage. As for most consumer products, the limited lifetime of this motor poses no problem, the only remaining problem for battery operated equipment is the high supply voltage. Hence, a converter is required with a high conversion ratio (e.g. a factor 10). If a simple topology like the boost converter would be used, this would imply operation with a very high duty ratio ($D > 0.9$), a very large VA-rating for the switches and a very low overall efficiency of the converter.

Similar problems exist for buck-type converters trying to accomplish very low conversion ratios (e.g. a factor 1/10). To avoid a very low duty ratio, quadratic buck converters with a conversion ratio proportional to D^2 have been reported [2–4]. The main disadvantages of these converters are the high component count, and the complexity of both the topology and the control strategy. Moreover, it is doubtful whether any of these quadratic buck converters can outperform a cascade of two buck converters when comparing overall system cost and efficiency. Driven by the demanding requirements of modern power-hungry microprocessors, new topologies have emerged [5,6]. By using coupled inductors, these converters are able to combine a low conversion ratio with a good efficiency and a moderate complexity.

A similar story applies to boost-type converters with a high conversion ratio. Converters with a quadratic or higher order conversion ratio [7] suffer from circuit complexity, high component count and low efficiency. To avoid these disadvantages boost converter topologies using a coupled inductor have been presented [8–11]. The main features of these converters are a high conversion ratio, a high efficiency, a single low-voltage active switch, a single inductive component, a low overall component count and a simple straightforward topology.

However, if the converter supplies a universal series motor for applications such as electrically assisted bicycles [1], the motor torque must remain controllable also at very low speeds. Consequently, the converter output should not only be capable of supplying high voltages, but also voltages lower than the input voltage.

In [9] it was shown that by making a small modification in the topology of the boost converter with coupled inductors, a buck-boost converter can be derived with a conversion ratio ranging from 0 to high values. As already demonstrated in [9], different variants for the buck-boost converter with coupled inductors exist. In this paper the different variants are discussed. From this analysis the optimum topology is chosen for converting a 24-V battery input into an output ranging from 0 V to 175 V. Experimental results show the high efficiency that can be reached with these type of converters.

II. Review of the Operating Principle of the Buck-Boost Converter with Coupled Inductors

The topology of the proposed converter is depicted in Fig. 1. This converter can be derived from the boost converter with coupled inductors depicted in Fig. 2 by moving the position of the load (represented by the resistor R). As the topology of this buck-boost converter is derived by a small modification of the boost converter presented in [8,9,11], the operating principle remains basically the same and is therefore reviewed only briefly. The buck-boost converter of Fig. 1 consists of a switch S_1, diodes D_1 and D_2, an intermediate capacitor C_1, an output capacitor C_2 and a transformer-inductor encompassed by the dashed line in Fig. 1. This transformer-inductor is characterized by the primary inductance L_1, the secondary inductance L_2, and the total leakage inductance $L_{\sigma 2}$ (here entirely assigned to the secondary). If the number of turns
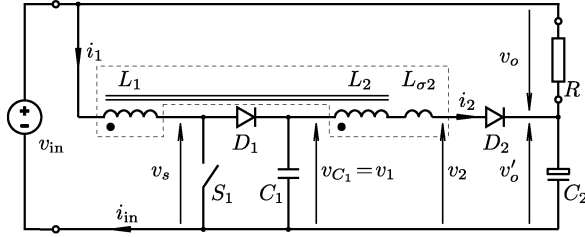
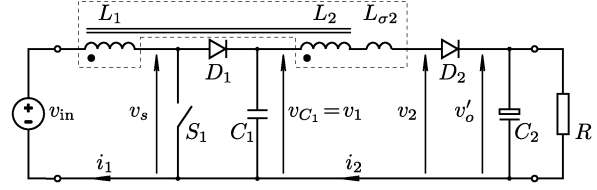Fig. 1. The proposed buck-boost converter with a high conversion ratio

Fig. 2. The boost converter with a high conversion ratio

in the primary and the secondary windings are n_1 and n_2, respectively, the following applies:

$$\frac{L_1}{L_2} = \left(\frac{n_1}{n_2}\right)^2. \tag{1}$$

The key waveforms of the buck-boost converter are shown in Fig. 3. The convertor is supplied from a dc source with a constant voltage v_{in}. The capacitors C_1 and C_2 are sufficiently large, so that the voltages v_{C_1} and v_o are virtually constant. Note that the output voltages of the boost converter (Fig. 2) and buck-boost converter (Fig. 1) are denoted with v_o' and v_o, respectively; both quantities are related by

$$v_o = v_o' - v_{\text{in}}. \tag{2}$$

Assume that right before time t_0 there exists a current $i_2(t_0)$ in diode D_2, while the current $i_1(t_0)$ in the primary of the coupled inductor is zero. At t_0 the switch S_1 is switched on and the voltage v_s across the switch S_1 becomes zero. Because of that, a voltage appears across the secondary of the transformer L_2 that decreases the current i_2 in diode D_2. Hence, between t_0 and t_1 the current in diode D_2 is commutating to the switch S_1. During this interval the diode D_2 is conducting and the voltage v_2 remains equal to the voltage v_o' (2). Due to the presence of the leakage inductance $L_{\sigma 2}$ of the transformer, the $\mathrm{d}i/\mathrm{d}t$ of the current i_2 is limited and the diode recovery losses of the diode D_2 are reduced. Moreover, the switch S_1 is switched on with zero current.

At time t_1, the current i_2 in the diode D_2 reaches zero and diode D_2 blocks. Between times t_1 and t_2, the voltage v_s across the switch S_1 remains zero and the current i_1 in the primary of the transformer rises. Meanwhile, the voltage v_2 is determined by the capacitor voltage v_{C_1} and the transformed primary voltage, or

$$v_2(t) = v_{C_1} - \frac{n_2}{n_1} v_{\text{in}} \qquad \text{for} \qquad t \in \,]t_1, t_2[. \tag{3}$$

As the diode D_2 remains reverse biased, the current i_2 remains zero during this time interval.

At time t_2, the switch S_1 is turned off very fast, the current is commutated to the parasitic output capacitance (C_{oss} for a MOSFET) of the switch S_1 (this short time interval is not shown in Fig. 3) and the voltage v_s ramps up quickly. Hence, the switch S_1 is switched off with zero voltage. As the following applies:

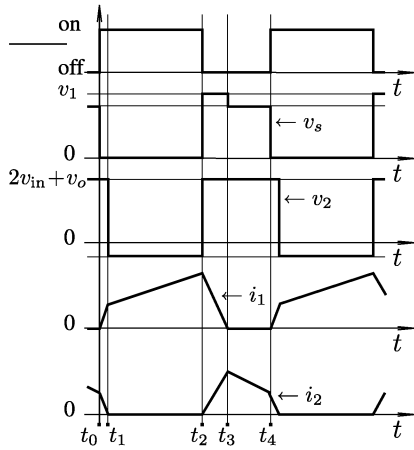$$\frac{v_o' - v_{C_1}}{n_2} < \frac{v_{C_1} - v_{in}}{n_1}, \tag{4}$$

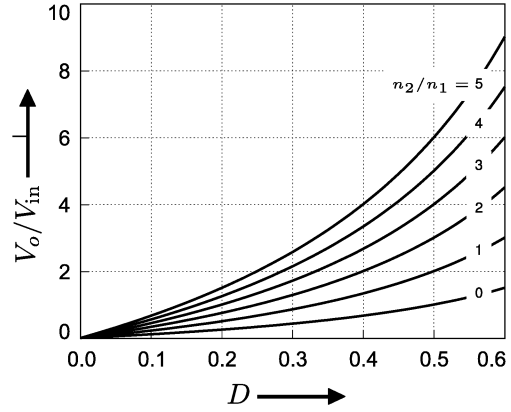Fig. 3. The key waveforms of the proposed buck-boost converter

Fig. 4. The conversion ratio of the proposed buck-boost converter as a function of the duty ratio D and the transformer turns ratio n_2/n_1

the current prefers to run in the secondary of the transformer, but is prohibited to commutate instantly by the leakage $L_{\sigma 2}$. Consequently, between time t_2 and t_3 both diodes D_1 and D_2 conduct current and the current i_1 is gradually commutating to the secondary of the transformer. Meanwhile, the switch voltage v_s is clamped to the capacitor voltage v_{C_1} and the voltage v_2 equals the voltage v'_o.

At time t_3, the current i_1 reaches zero and diode D_1 is blocked. All the current is commutated to the secondary of the transformer and is used to charge the output capacitor through the diode D_2. Between t_3 and t_4, the switch voltage v_s is

$$v_s = v_{in} + \frac{n_1}{n_2}(v'_o - v_{C_1}) < v_{C_1}, \tag{5}$$

a voltage slightly smaller than the voltage v_{C_1}. Eventually, at time t_4 the starting situation (at time t_0) is reached again.

If the leakage inductance $L_{\sigma 2}$ of the transformer is small, the conversion ratio of the proposed buck-boost converter can be derived by combining (2) with the conversion ratio reported in [11] for the boost converter

$$\frac{v_o}{v_{in}} \approx \frac{n_2}{n_1} \cdot \frac{D}{1-D}, \tag{6}$$

with D the duty ratio of the switch S_1. The voltage across the intermediate capacitor C_1 remains unchanged as compared to the boost topology. Hence, this formula can be copied from [11]:

$$\frac{v_{C_1}}{v_{in}} \approx \frac{1}{1-D}. \tag{7}$$

The conversion ratio of the buck-boost converter (6) is shown in Fig. 4 as a function of the duty ratio D and the turns ratio n_2/n_1 of the transformer. Note that if the turns ratio n_2/n_1 is chosen equal to zero ($n_2=0$), the topology (Fig. 2) and the conversion ratio (Fig. 3) of the "regular" buck-boost converter are obtained. For transformer turns ratios $n_2/n_1 \geq 1$, high conversion ratios can be achieved, while the duty ratio D remains smaller than 0.6 (This duty-ratio range is favourable as it provides a good silicon usage and a high efficiency at full load.). Moreover,
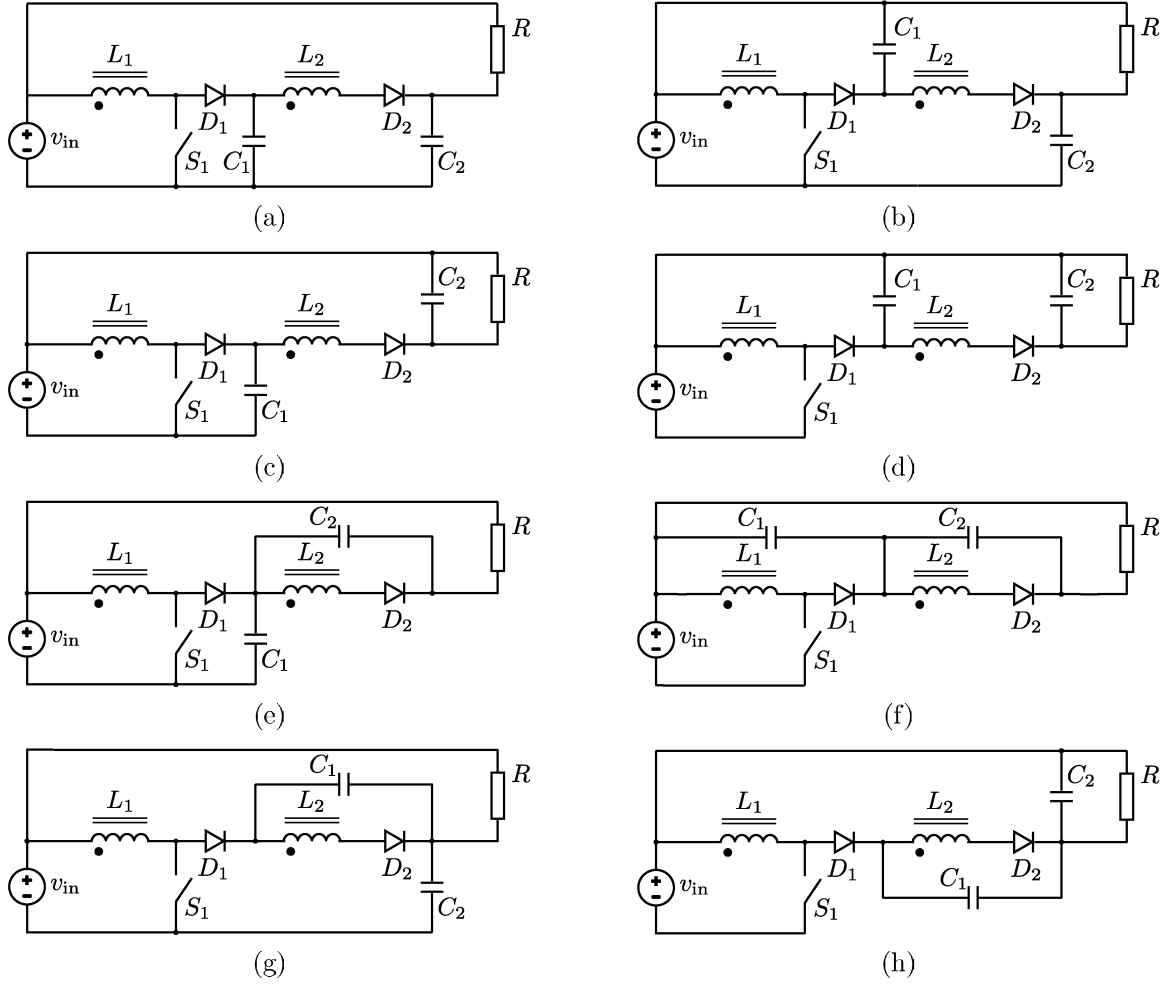
Fig. 5. Different topological variations of the buck-boost converter with coupled inductors

the voltage across the capacitor C_1 remains independent of the turns ratio of the transformer (7). Consequently, a low-voltage switch S_1 and a low-voltage diode D_1 can be chosen, though the output voltage v_o can be up to 10 times higher than the input voltage v_{in}.

In the case where the leakage inductance $L_{\sigma 2}$ cannot be neglected, the conversion ratios in the converter become load dependent. In general, the output voltage v_o sets with increasing load current and is slightly lower than the value predicted by (6). On the contrary, the voltage v_{C_1} across the intermediate capacitor rises with increasing load current and becomes slightly larger than stated by (7).

III. The Different Topological Variations

The two capacitors C_1 and C_2 in the topology of Fig. 1 can be connected to different nodes without altering the principles of operation of the converter. The different possibilities result in 8 different topological variations of the buck-boost converter with coupled inductors Fig. 5. Three of these topological variants, viz Figs. 5(c), 5(d) and 5(h), were published before in [9]. So as to decide which variant is best suited for the application, several properties of the different topological variations are studied.
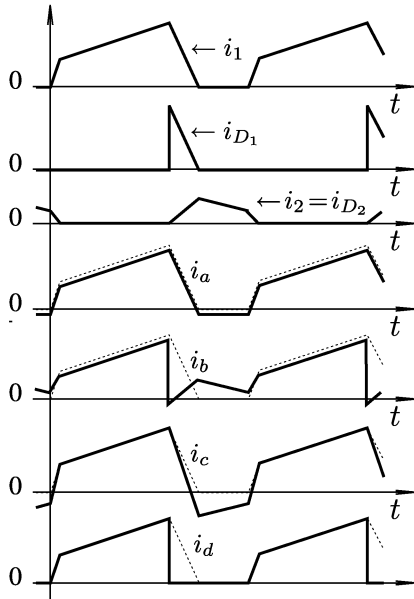
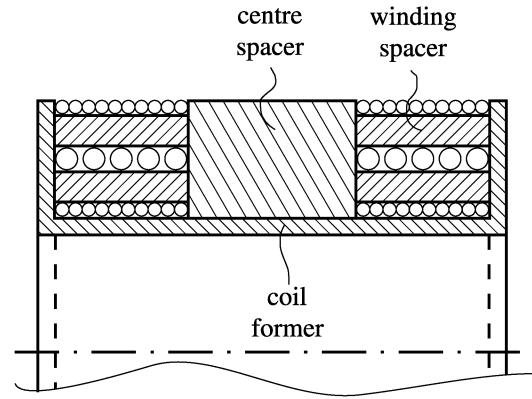Fig. 6. The input current waveforms of the different topological variations

Fig. 7. The winding construction in the transformer-inductor

A. Input Current

An important property of a topology is its input current[1] waveform. The different input currents for the different variants are shown in Fig. 6 (the current in the primary of the transformer i_1 is added as a dotted line for comparison). In this figure four different input current waveforms can be distinguished:

1. $i_{in} = i_a = i_1 - i_R$: (i_R is the dc current through the load R) This input current waveform belongs to the variants of Figs. 5(a), 5(e) and 5(g), and is characterized by a relatively low rms value and by the limited values of the di_{in}/dt. A disadvantage of this current waveform is that during a significant interval of time current is flowing back to the source.
2. $i_{in} = i_b = i_1 - i_{D_1} + i_2 - i_R$: This input current waveform applies only for Fig. 5(b). The rms value of the input current is the lowest of all variants of this topology. However, the slope of the current is very high when switch S_1 is switched off. The input current becomes negative only during a very small interval of time every switching period.
3. $i_{in} = i_c = i_1 - i_2$: The converter of Fig. 5(c) has an input current waveform like i_c in Fig. 6. The current slope is also limited in this case, but slightly higher than for the current i_a of case 1. However, the rms value of the current is the highest of all four cases. This is also the current waveform with the largest portion of current flowing back to the supply.
4. $i_{in} = i_d = i_1 - i_{D_1}$: The input current i_d applies to the cases of Figs. 5(d), 5(f), and 5(h). The rms value is higher compared to cases 1 and 2, but lower than for case 3. The slope of the input current is again high. These topological variants are the only ones with a current waveform that remains positive over the entire switching period.

B. Capacitor Voltage Rating

The maximum voltage rating of a capacitor is in most cases determinative for the price and size of this passive component. Depending on the topology, three different values for the maximum voltage $V_{C_1}^{max}$ of the capacitor C_1 are possible:

---

[1]The input current is the current i_{in} supplied by the source v_{in}.

1. $V_{C_1}^{\mathrm{max}} = \frac{D}{1-D}v_{\mathrm{in}}$: This lowest possible voltage rating applies to the topologies of Figs. 5(b), 5(d), and 5(f).

2. $V_{C_1}^{\mathrm{max}} = \frac{1}{1-D}v_{\mathrm{in}}$: The intermediate $V_{C_1}^{\mathrm{max}}$ rating belongs to the topologies of Figs. 5(a), 5(c), and 5(e). If the duty ratio D is limited to e.g. 0.6, this voltage rating is 66.7% higher than the rating of case 1.

3. $V_{C_1}^{\mathrm{max}} = \frac{n_2}{n_1}\frac{1}{1-D}v_{\mathrm{in}}$: In most cases the number of secondary turns n_2 is larger than the number of primary turns n_1. For a transformer turns-ratio of 4 and a duty ratio lower than 0.6, the maximum voltage across C_1 can adopt values that are 566.7% higher than in case 1. The topologies of Figs. 5(g) and 5(h) suffer from this very high voltage rating for capacitor C_1 and are therefore less favourable.

For capacitor C_2 three different voltage ratings are also possible. However, the difference between the distinct cases is less pronounced than for capacitor C_1. The different cases are:

1. $V_{C_2}^{\mathrm{max}} = \frac{n_2}{n_1}\frac{1}{1-D}v_{\mathrm{in}}$: The lowest possible voltage rating for capacitor C_2 applies to Figs. 5(e) and Figs. 5(f).

2. $V_{C_2}^{\mathrm{max}} = \left(D + \frac{n_2}{n_1}\right)\frac{1}{1-D}v_{\mathrm{in}}$: For a transformer turns-ratio of 4 and duty ratio D limited to 0.6, this value is 15% higher compared to case 1. The topologies of Figs. 5(c), 5(d), and 5(h) display such a voltage rating.

3. $V_{C_2}^{\mathrm{max}} = \left(1 + \frac{n_2}{n_1}\right)\frac{1}{1-D}v_{\mathrm{in}}$: This last rating is 50% higher compared to case 1, and is valid for Figs. 5(a), 5(b), and 5(g).

As the voltage ratings of capacitor C_2 only mildly varies over the different topologies, no specific topology can be rejected solely based on this last rating.

C. Capacitor Current Rating

The rms current ratings for the capacitors C_1 and C_2 vary only slightly over the different topologies of Figs. 5(a)–(f). In all these topologies the rms current for C_1 is much larger than that for C_2. However, for the topologies of Figs. 5(g) and 5(h), the current rating for capacitor C_2 is approximately equal to that for C_1 and, hence, much higher compared to the other variants. Based on the required high voltage rating for C_1 (previous subsection), and the high rms current rating for capacitor C_2, the topologies of Figs. 5(g) and 5(h) can in most cases be rejected beforehand.

D. Output Voltage Ripple

The output voltage ripple Δv_o is for most variants determined by the impedance value of the output capacitor C_2 and the ripple present on the dc supply v_{in}. As in most cases a significant voltage ripple is allowable across C_1, the capacitance value of this capacitor may be chosen rather low. However, because of the series connection of the capacitors C_1 and C_2 in the topologies of Figs. 5(e) and 5(f), the voltage ripples of both capacitors add up. Hence, for these two topologies, C_1 must also have a significantly large capacitance value, if a low output voltage ripple is desired.

E. Choice of Variant

Based on the above criteria, the best-suited topology for a certain application can be chosen. In our case a converter was required for the supply of a universal series motor from a battery input. Topologies (g) and (h) are rejected because of the high rms current rating of capacitor C_2. Based
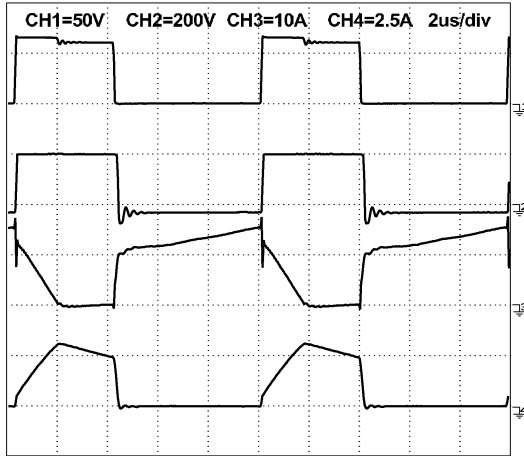
Fig. 8. Experimental waveforms of the proposed buck-boost converter: (from top to bottom) switch voltage v_s, voltage v_2, primary current i_1, and secondary current i_2
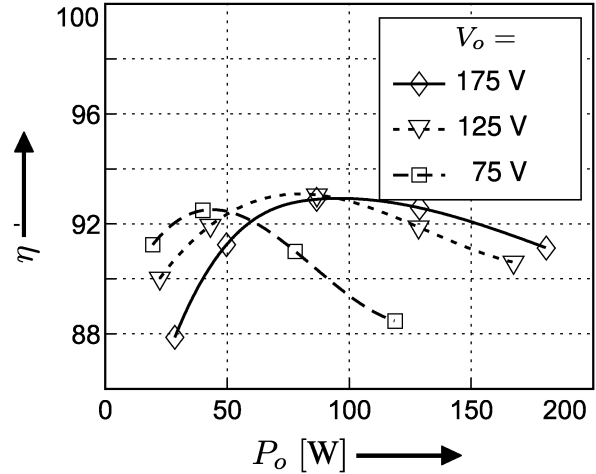
Fig. 9. The efficiency η of the proposed buck-boost converter as a function of the output voltage V_o and the output power P_o

on the criterion of capacitor voltage rating, the topological variant (f) is the absolute favourite, with the lowest voltage ratings for both capacitors C_1 and C_2. However, the voltage rating of capacitors can only adopt certain values predefined by the manufacturers. As a result, the voltage ratings of the capacitor sometimes may be significantly larger than the theoretically required value, allowing for another topological variant with a somewhat higher required capacitor voltage rating. Therefore, topological variant (b) is chosen finally. Though this topological variant suffers from a 50% higher required voltage rating for capacitor C_2, the rms value of the input current is the lowest possible.

IV. Experimental Results

To test the theoretical behaviour of the proposed buck-boost converter, a 175-W prototype was built, converting a 24-V battery input into a 175-V output. Hence, for this prototype a conversion ratio of approximately 7.3 is required. The conversion-ratio graph (Fig. 4) shows that for duty ratios lower than 0.6, the turns ratio of the transformer should be 4, at least. For the prototype, the minimum required turns ratio of 4 was chosen. The converter is switched at 100 kHz. As a significant ripple is allowable on the intermediate voltage v_{C_1}, the capacitor C_1 has a relatively low capacitance of 10 μF (a polyester film capacitor rated for 100 V). This converter is designed to supply a universal series motor. Hence, a relatively high output-voltage ripple is allowable. Therefore, a 1 μF / 250 V polyester film capacitor was chosen for the output capacitor C_2. The primary and secondary inductances of the transformer-inductor are $L_1 = 26.5$ μH and $L_2 = 419$ μH, respectively.

The transformer-inductor was constructed with an ETD39 core of 3C85 material. As the $\mathrm{d}i/\mathrm{d}t$ of the commutating currents is mainly determined by the leakage inductance $L_{\sigma 2}$ of the transformer-inductor, the leakage inductance was maximized. Fig. 7 shows a cross-section of the construction of the transformer-inductor. To avoid proximity losses in the wires caused by the fringing field around the centre gap in the core material (core is not shown in Fig. 7), a cylindrical centre spacer (10 mm wide) is added on the coil former. The primary winding consists of a single layer with 10 turns of 1.2 mm wire, which is sandwiched between two layers of the secondary winding. The secondary winding consists of a total of 40 turns of 0.71 mm copper wire. To increase the leakage inductance without adverse effects on the proximity losses, the

inter-winding space is increased by inserting a cylindrical winding spacer (2 mm thick) between the different winding layers. The resulting leakage inductance is $L_{\sigma 2} = 12.9$ μH.

For the switch S_1, a 100 V MOSFET was used with $R_{\mathrm{ds(on)}} = 0.023$ Ω: FQP70N10 of Fairchild Semiconductor. As the maximum blocking voltage for diode D_1 is below 70 V, a 100 V schottky diode (50WQ10FN of International Rectifier) was used (by using a schottky diode the conduction losses are decreased). Although the rate of change of the current i_2 is limited by the leakage, it still remains significant ($-\mathrm{d}i_2/\mathrm{d}t \approx 25$ A/μs) between t_0 and t_1 (Fig. 3). Therefore, a new Gallium-Arsenide schottky diode (DGS3-030AS) of IXYS was used with a blocking voltage of 300 V and a current rating of 3 A.

The voltage waveforms of the converter at full load are depicted in Fig. 8. The waveforms show a good agreement with the theoretical waveforms of Fig. 3. For this experiment the duty ratio of the switch S_1 was set to 0.6. The converter delivered 175 W to its 175-V output, while the capacitor voltage V_{C_1} stayed at 66 V. Note that both (6) and (7) are approximately fulfilled.

Finally, the efficiency η for the converter was tested as a function of the output power P_o and for different output voltages V_o. The results are depicted in Fig. 9. The efficiency of the converter peaks at 93% and remains above 90% for a wide output-power range and output-voltage range. (The measurement for 175 W at 75 V was omitted because this load condition exceeds the power rating for the diode D_2 in the prototype.)

V. Conclusion

To supply a high voltage load from a low voltage source, a converter with a high conversion ratio is required. If the load power needs to be controlled down to 0, this converter must often be capable of also supplying output voltages lower than the input voltage. Converter topologies that fulfil these requirements, have been presented before. One of the topologies that catches the eye due to its straightforward topology and its high efficiency is the buck-boost converters with coupled inductors. However, if all the different locations of the capacitors in this topology are considered, different topological variants can be derived. In this paper, the topological variants are compared based on their different properties. The resulting criteria allow to choose the right topology starting from the load requirements. Finally, a topology is chosen for the supply of a universal series motor from a low voltage battery. Experimental results show that this converter can attain a high efficiency over a wide output-power range and output-voltage range.

References

[1] A.P. Van den Bossche, K. De Gussemé, and J.A. Melkebeek, ZVZC dc-dc converter for electrical bike using a 230V series motor, *Proc. of the 10th Eur. Conf. on Power Electr. and Applic.*, EPE 2003, Sept. 2-4, 2003, Toulouse, France, on CD-rom.

[2] V.M. Pacheco, A.J. do Nascimento, V.J. Farias, J.B. Vieira, and L.C. de Freitas, "A quadratic buck converter with lossless commutation," *IEEE Trans. Ind. Electr.*, Vol. 47, No. 2, pp. 264–272, Apr. 2000.

[3] D. Maksimović, S. Ćuk, "Switching converters with wide dc conversion range," *IEEE Trans. Power Electr.*, Vol. 6, No. 1, pp. 151–157, Jan. 1991.

[4] L. dos Reis Barbosa, J.B. Vieira, L.C. de Freitas, M. da Silva Vilela, V.J. Farias, "A buck quadratic PWM soft-switching converter using a single active switch," *IEEE Trans. Power Electr.*, Vol. 14, No. 3, May 1999.

[5] T.H. Kim, J.H. Park, and B.H. Cho, "Small-signal modeling of the tapped-inductor converter under variable frequency control," *Proc. of the 35th IEEE Power Electr. Spec. Conf.*, PESC04, Aachen, Germany, 2004, pp. 1648–1652.

[6] K. Yao, Y. Ren, J. Wei, M. Xu, and F.C. Lee, "A family of buck-type dc-dc converters with autotransformers," *Proc. of the 2003 IEEE Appl. Power Electr. Conf.*, APEC03, Miami, USA, Feb. 9–13, 2003, pp. 114–120.

[7]   F.L. Luo, and H. Ye, "Positive output cascade boost converters," *IEE Proc.-Electr. Power Appl.*, Vol. 151, No. 5, pp. 590–606, Sept. 2004.

[8]   Q. Zao, and F.C. Lee, "High performance coupled-inductor dc-dc converters," *Proc. of the 2003 IEEE Appl. Power Electr. Conf.*, APEC03, Miami, USA, Feb. 9–13, 2003, pp. 109–113.

[9]   Q. Zhao, and F.C. Lee, "High efficiency, high step-up dc-dc converters," *IEEE Trans. Power Electr.*, Vol. 18, No. 1, Jan. 2003, pp. 65–73.

[10] T.J. Liang, and K.C. Tseng, "Analysis of integrated boost-flyback step-up converter," *IEE Proc.-Electr. Power Appl.*, Vol. 152, No. 2, Apr. 2005, pp. 217–225.

[11] D.M. Van de Sype, K. De Gussemé, B. Renders, A.P. Van den Bossche, and J.A. Melkebeek, "A single switch boost converter with a high conversion ratio," *IEEE Applied Power Electronics Conference*, APEC2005, Austin, Texas, USA, March 6–10, 2005, pp. 1581–1587.