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A new quantum-dot cellular automata full-adder

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ABSTRACT

A novel expandable five-input majority gate for quantum-dot cellular automata and a new full-adder cell are presented. Quantum-dot cellular automata (QCA) is an emerging technology and a possible alternative for semiconductor transistor based technologies. A novel QCA majority-logic gate is proposed. This component is suitable for designing QCA circuits. The gate is simple in structure and powerful in terms of implementing digital functions. By applying these kinds of gates, the hardware requirement for a QCA design can be reduced and circuits can be simpler in level, gate counts and clock phases. In order to verify the functionality of the proposed device, some physical proofs are provided. The proper functionality of the FA is checked by means of computer simulations using QCADesigner tool. Both simulation results and physical relations confirm our claims and its usefulness in designing every digital circuit.

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1. Introduction

Current CMOS technology is going to approach a scaling limit in deep nanometer technologies. The CMOS technology in nano-scales has some problems because of increase in amounts of variation in every aspect of a nanometer design. One conventional way to enhance the performance of logical systems is to use parallelism [1,2]. But in order to enhance the overall performance of the system new nanotechnologies must be taken into account. Quantum-dot cellular automata (QCA) is one of the promising new technologies that not only gives a solution at nano-scale, but also it offers a new method of computation and information transformation [3,4]. The basic building block of QCA circuit is majority gate; hence, efficiently constructing QCA circuits using majority gates has attracted a lot of attentions, but some of them are not realizable or not expandable [5,7]. Several studies have reported that QCA can be used to design general purpose computational and memory circuits [8]. Since every QCA circuit can be implemented only using majority and inverter gates, another important component in constructing QCA circuits is the inverter. Hence, efficiently constructing an inverter in QCA is of great importance [6].

As already mentioned, the basic building block of QCA circuit is majority gate; majority logic is a way of implementing digital operations in a manner different from that of Boolean logic.

Instead of using Boolean logic operators (AND, OR and their complements), majority logic represents and manipulates digital functions on the basis of majority decision [9]. The logic process of majority logic is more sophisticated than that of Boolean logic; consequently, majority logic is more powerful for implementing a given digital function with a smaller number of logic gates [10,11].

In this paper, we propose a new design for majority gates resulting in simplification of logical functions. By applying this form of majority gate, we can simplify logical functions and achieve improved results. The presented method is justified based on physical relation proofs as well as simulation results. In comparison to other existing implementations, this method has demonstrated significant improvements. The proposed majority gate resulted in decrease in gate counts and levels in QCA designs. One of the most important components in every arithmetic and digital circuits in QCA and VLSI is full-adder [7,12,13].

To demonstrate the efficiency of the proposed gate, a QCA full-adder is implemented using the new presented majority gate. Comparisons show that the new full-adder is more efficient in terms of cell counts, complexity and area in comparison to other previous state-of-the-art designs [4,7,14–17].

2. Materials and methods

2.1. Background

Quantum cellular automata is a new device architecture, which is proper for the nanometer scale [18]. The principle of QCA was first proposed by Lent and Tougaw [18]. A quantum cell can be

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viewed as a set of four charge containers or dots, positioned at the corners of a square. The cell contains two extra mobile electrons, which can quantum mechanically tunnel between dots but not cells [4,19]. The electrons are forced to the corner positions by Coulombic repulsion. The two possible polarization states represent logic “0” and logic “1”, as shown in Fig. 1(a) [4,20].

As shown in Fig. 1(b), an ordinary QCA gate implementing the majority function is as follows:

Assuming three inputs labeled A, B and C, the logic function of majority gate is

$$M(A,B,C) = AB + AC + BC \quad (1)$$

Besides, truth table of a three-input majority gate is shown in Table 1. As illustrated in Fig. 1(b) each QCA majority gate in normal form requires only five QCA cells. And in Fig. 1(c) a QCA inverter is shown.

2.2. Five-input majority gate

A five pins majority gate must have five inputs and one output. A truth table of a five-input majority gate based on sum of inputs is shown in Table 2.

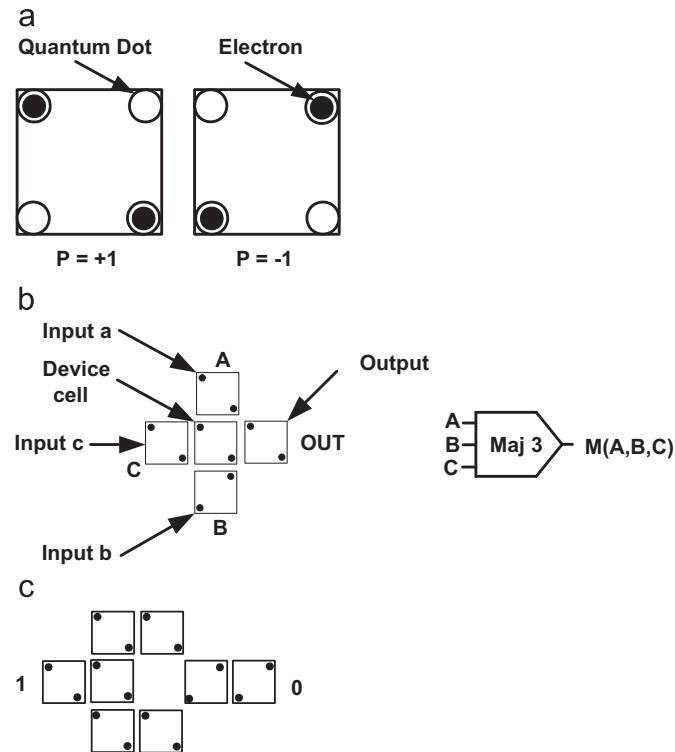


Fig. 1. (a) Basic QCA cell and binary encoding, (b) A QCA majority gate and (c) A QCA inverter.

Table 1
Truth table of a three-input majority gate.

A	B	C	M(A,B,C)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 2

Truth table of a five-input majority gate based on sum of inputs.

$\sum (A,B,C,D,E)$	$M(A,B,C,D,E)$
0	0
1	0
2	0
3	1
4	1
5	1

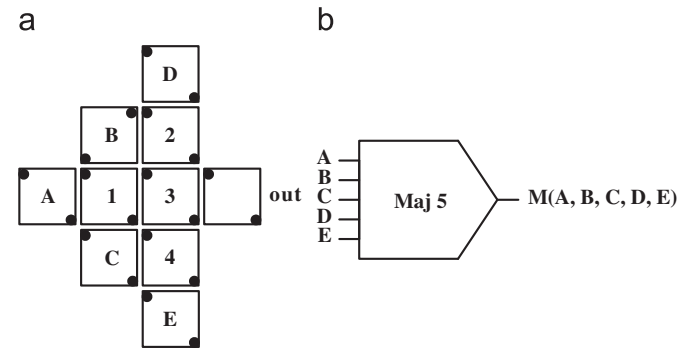


Fig. 2. (a) Proposed five-input majority gate and (b) Schematic symbol for the majority gate.

Majority is a voter. In our new structure, a majority gate can be implemented as shown in Fig. 2(a). In this scheme we have five inputs labeled A, B, C, D and E and the output cell is shown by out. In addition, four middle cells labeled 1, 2, 3 and 4. Polarization of input cells is fixed and middle cells and output cell are free to change.

In this design the input cell A only has an effect on middle cell 1. Also, the input cells B and C have only effect on 1, 2, 3 and on 1, 3, 4 middle cells, respectively. In a similar manner, the input cells D and E have effect on middle cells 2 and 4. Through these effects, the majority decision of inputs is transferred to the output and constructs the five-input majority gate, efficiently.

The majority voting logic function can be expressed in terms of fundamental Boolean operator as shown in

$$M(A,B,C,D,E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \quad (2)$$

A schematic symbol of a five-input majority gate is shown in Fig. 2(b). We can implement a three-input AND gate and also a three-input OR gate using this majority gate. These functions are as

$$M(A,B,C,0,0) = ABC \quad (3a)$$

$$M(A,B,C,1,1) = A + B + C \quad (3b)$$

As it is clear in Fig. 2(a), a five-input majority gate only needs ten cells and by considering some physical relations it is implemented.

Regarding the physical proofs, assume that all cells are similar and the length of each one is a ($a = 18$ nm) and there is a space of x ($x = 2$ nm) between each two neighbor cells.

In all figures, rectangles show a QCA cell and the circles inside show the electrons inside that cell. It should be noted that in order to achieve more stability, electrons of QCA cell are arranged in such a manner that their potential energy reaches the minimum level.

The potential energy between two electron charges is calculated using relation (4a). In this equation, U is the potential

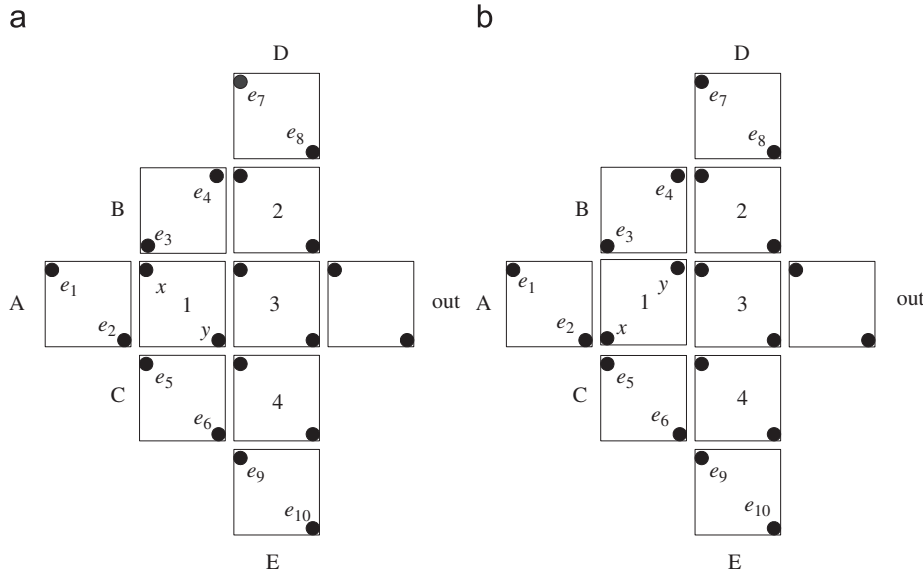


Fig. 3. (a) The one value in cell 1 and (b) The zero value in cell 1.

energy, k is fixed colon, q_1 and q_2 are electric charges and r is the distance between two electric charges. By putting the values of k and q , we obtain Eq. (4b). U_T is the summation of potential energies that is calculated from Eq. (5) [21–23].

$$U = \frac{kq_1q_2}{r} \quad (4a)$$

$$kq_1q_2 = 9 \times 10^9 \times (1.6)^2 \times 10^{-38} = 23.04 \times 10^{-29} = A = cte \quad (4b)$$

$$U_T = \sum_{i=1}^n U_i \quad (5)$$

Fig. 3(a) (electron x)

$$U_1 = \frac{A}{r_1} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} \approx 1.15 \times 10^{-20} \text{ J}$$

$$U_2 = \frac{A}{r_2} = \frac{23.04 \times 10^{-29}}{18.11 \times 10^{-9}} \approx 1.27 \times 10^{-20} \text{ J}$$

$$U_3 = \frac{A}{r_3} = \frac{23.04 \times 10^{-29}}{2 \times 10^{-9}} \approx 11.52 \times 10^{-20} \text{ J}$$

$$U_4 = \frac{A}{r_4} = \frac{23.04 \times 10^{-29}}{26.91 \times 10^{-9}} \approx 0.86 \times 10^{-20} \text{ J}$$

$$U_5 = \frac{A}{r_5} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} \approx 1.15 \times 10^{-20} \text{ J}$$

$$U_6 = \frac{A}{r_6} = \frac{23.04 \times 10^{-29}}{42.04 \times 10^{-9}} \approx 0.55 \times 10^{-20} \text{ J}$$

$$U_{T11} = \sum_{i=1}^6 U_i = 16.5 \times 10^{-20} \text{ J}$$

$$U_{T1} = \sum_{i=1}^2 U_{1i} = 22.09 \times 10^{-20} \text{ J}$$

potential energy (U_T) in both states using Eq. (5). The comparison of total potential energies in both (a) and (b) states shows which state (a or b) is more stable. The state that has the lower potential energy level is the one which is more suitable for us. With determining the value of cell 1 and considering input cells B and C the values of cell 2 and 4 can be simultaneously computed in a similar manner to that for cell 1. Then, with having all values of cells 1, 2 and 4 and also with considering cells B and C, which have a diagonal effect on cell 3, the value of this cell can be computed and this result is transferred to the output cell, which give us a majority decision of inputs A, B, C, D and E.

As the proof method is similar for all cells and their values, only the first part of this proof is stated and the rest of relations are omitted due to lack of space. (Fig. 3)

Fig. 3(a) (electron y)

$$U_1 = \frac{A}{r_1} = \frac{23.04 \times 10^{-29}}{42.04 \times 10^{-9}} \approx 0.55 \times 10^{-20} \text{ J}$$

$$U_2 = \frac{A}{r_2} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} \approx 1.15 \times 10^{-20} \text{ J}$$

$$U_3 = \frac{A}{r_3} = \frac{23.04 \times 10^{-29}}{26.91 \times 10^{-9}} \approx 0.86 \times 10^{-20} \text{ J}$$

$$U_4 = \frac{A}{r_4} = \frac{23.04 \times 10^{-29}}{38 \times 10^{-9}} \approx 0.61 \times 10^{-20} \text{ J}$$

$$U_5 = \frac{A}{r_5} = \frac{23.04 \times 10^{-29}}{18.11 \times 10^{-9}} \approx 1.27 \times 10^{-20} \text{ J}$$

$$U_6 = \frac{A}{r_6} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} \approx 1.15 \times 10^{-20} \text{ J}$$

$$U_{T12} = \sum_{i=1}^6 U_i = 5.59 \times 10^{-20} \text{ J}$$

Since cells D and E are in a roughly long distance from cell 1, their potential energy can be neglected.

Fig. 3(b) (electron x):

$$U_{T21} = \sum_{i=1}^6 U_i = 26.46 \times 10^{-20} \text{ J}$$

$$U_{T2} = \sum_{i=1}^2 U_{2i} = 31.82 \times 10^{-20} \text{ J}$$

Fig. 3(b) (electron y):

$$U_{T22} = \sum_{i=1}^6 U_i = 5.36 \times 10^{-20} \text{ J}$$

With comparison of the achieved results, the electrons in cell 1 are positioned in state (a) because this state is more stable and

2.3. Physical proof

As a five-input majority gate has 32 different input states, we should check all the states to verify the correctness of the gate. Here, only one state ($A=1, B=0, C=D=E=1$) is proved and the other states can be proved as well.

First, we calculate the potential energy existing between each electron (e_1, e_2, e_3, e_4, e_5 and e_6) with electrons “ x ” and “ y ” in (a) and (b) states using (4a) and (4b) equations. For example U_i is the potential energy existing between electron e_i and x (or y). Also, r_i is the distance between two electron charges. Then we calculate the total

has a lower potential energy. As already mentioned, the computation of potential energies for other cells (2, 3 and 4) is similar to those which have done for cell 1 and only the final results are mentioned. It is worth mentioning that in all cells U_{T_1} is the potential energy in +1 polarization and U_{T_2} is the potential energy in -1 polarization.

cell 2:	cell 3:	cell 4:
$U_{T_1} = 20.79 \times 10^{-20}$ J	$U_{T_1} = 12.36 \times 10^{-20}$ J	$U_{T_1} = 17.94 \times 10^{-20}$ J
$U_{T_2} = 21.35 \times 10^{-20}$ J	$U_{T_2} = 41.55 \times 10^{-20}$ J	$U_{T_2} = 31.09 \times 10^{-20}$ J

Considering the above computing, we can infer that the proposed structure for implementing a five-input majority gate is completely true and resulted in a correct state for the output cell, which shows the majority decision.

After physical proof, we can also check the proposed design using QCADesigner. Simulation of this majority gate is shown in Section 4. The next section shows the use of the new majority gate for implementing a full-adder.

3. One bit QCA full-adder

The proposed majority design is applied to implement a QCA full-adder. First, other QCA implementations of full-adders are presented and then our design is introduced. A one-bit full-adder is defined as follows:

Inputs: operand bits (A, B) and carry bit is shown as C.
Outputs: Sum and Carryout.

3.1. A QCA full-adder with seven gates

In a classic design in [4], a full-adder with five, three-input majority gates and three inverters has been implemented. We can simplify this design and reduce one majority gate simply. Thus, an easier form for this QCA full-adder can be implemented using four majority gates and three inverters (Fig. 4).

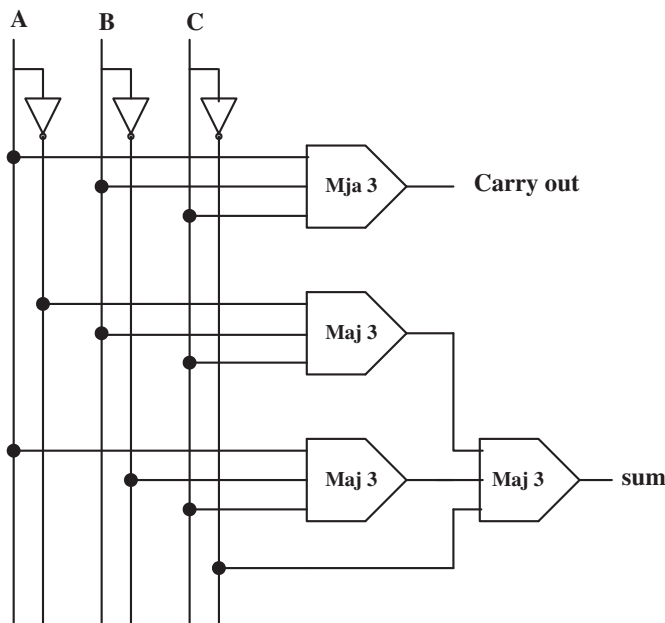


Fig. 4. One-bit QCA full-adder with seven gates.

It should be noted that in this design, a one-bit full-adder is implemented using only inverters and majority gates, whereas in order to implement the sum function based on AND/OR implementation, the number of gates involved will be increased.

3.2. A QCA full-adder with five gates

In [14] a method for decreasing the number of majority gates for QCA circuits has been presented and another form of QCA full-adder is expressed. In this design there are three three-input majority gates and two inverters (Fig. 5). It is worth mentioning that layout of this full-adder has four clocking phases.

3.3. A QCA full-adder with three gates

In one of the last design, a QCA full-adder is implemented only using three gates, two majority gates and one inverter (Fig. 6). Although this design has used an unconventional form of majority gates, a gate with five inputs, it has a simpler design scheme in comparison to other previous design [7]. In this study, authors have introduced a new design for QCA cells to implement their proposed majority design. This new cell has a cubic structure and maybe it is not simply feasible to fabricate. Although these kinds of cells seem too hard to be implemented, the idea of five-input majority gates is worth considering.

3.4. A QCA full-adder with five gates and three clocks

Recently, another design is presented which introduce a new design for QCA full-adders [15]. This design is the so-called carry flow adder (CFA), which revised the previous full-adder scheme. The schematic of this design is shown in Fig. 7.

This design has only three clock phases and also has a lower number of cells in comparison to all previous designs.

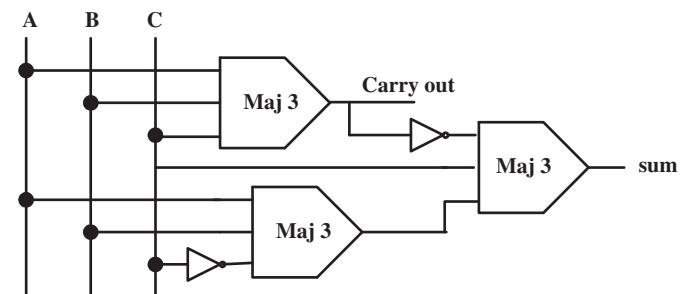


Fig. 5. One-bit QCA full-adder with five gates.

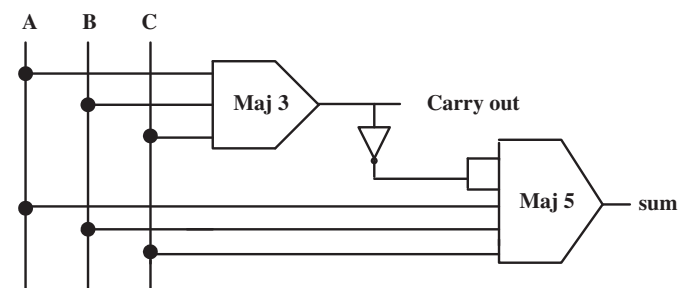


Fig. 6. One-bit QCA full-adder with three gates.

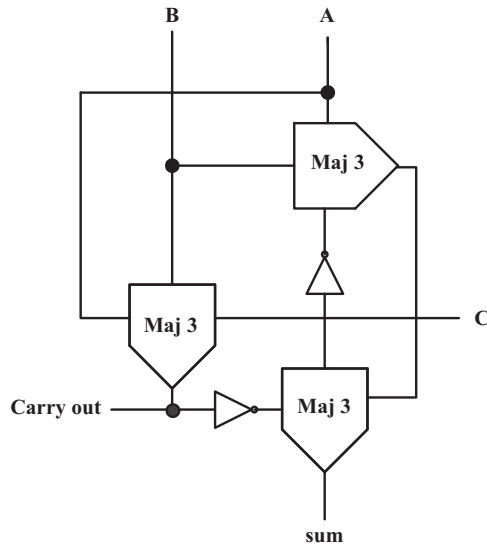


Fig. 7. One-bit QCA full-adder with five gates and three clocks.

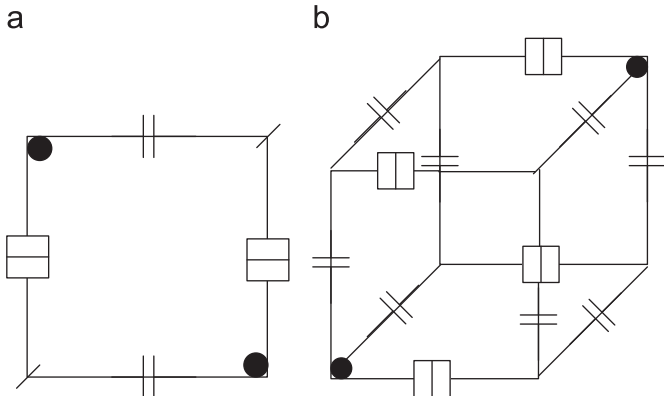


Fig. 8. (a) A QCA cell and (b) SEB structure.

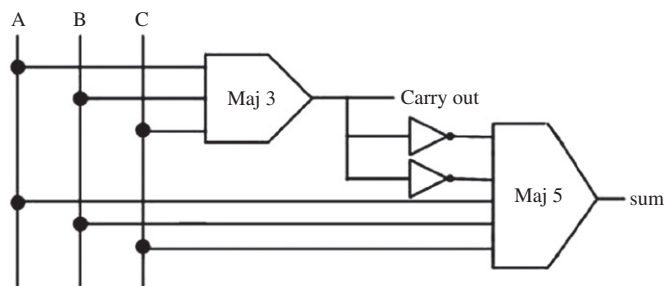


Fig. 9. Schematic design of the proposed full-adder with two majority gates and two inverters.

3.5. Proposed QCA full-adder

As already mentioned, in order to implement a new five-input majority gate, a new structure is introduced in this paper. This design realizes a five-input majority gate in a planar structure (Fig. 2). By means of this new five-input majority gate, a new and efficient full-adder is designed. The schematic design of the proposed full-adder is presented in Fig. 9. In addition, Fig. 10 illustrates the layout of the proposed full-adder, which uses a planar five-input majority gate. Although the proposed logic

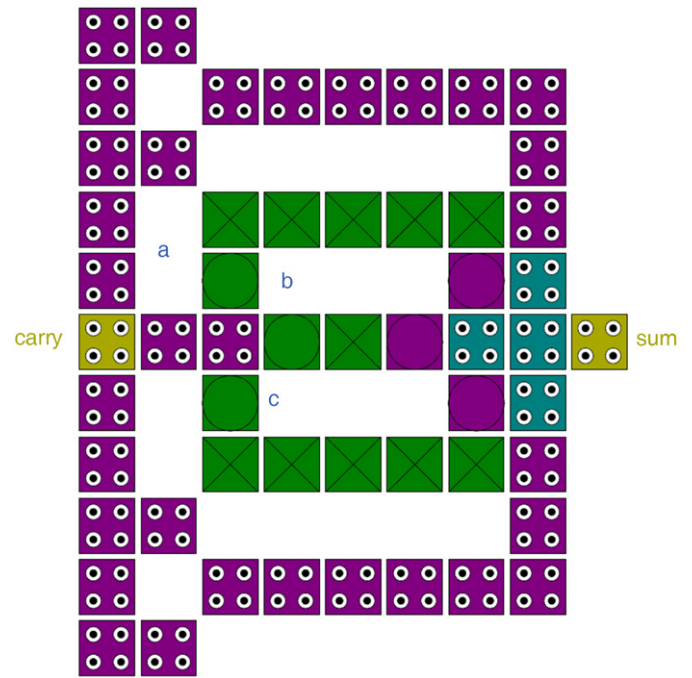


Fig. 10. Layout of the proposed full-adder in three layers and using three clock phases.

diagram for the full-adder in this paper uses two inverters and two majority gates and in comparison with the previous design (Fig. 6) in [7], it has one more inverter gate, the efficient layout of the new schematic worth tolerating one more inverter gate. Because of the new design for five-input majority gate, it would be better to use two inverters rather than one inverter and some wires for transferring inverted values to another point. Also, the previous design uses single electron box (SEB) structure that consists of two cells and four capacitors. In the proposed design, we used conventional form of cells that has an efficient layout to be simply fabricated. Fig. 8 shows the differences between QCA cell and SEB structure.

The proposed full-adder is implemented only using conventional cells and in three layers. It has 73 cells and it longs three clock phases to generate correct outputs (Sum and Carryout). In comparison to other previous design this full-adder resulted in significant improvements in terms of area, complexity and has a similar structure in terms of delay. Simulation results section compares all previous designs and shows the prosperity of the new presented design.

4. Simulation and practical results

For the proposed circuit layout and functionality checking, a simulation tool for QCA circuits, QCADesigner version 2.0.3 [24], is used. The following parameters are used for a bistable approximation: cell size=18 nm, number of samples=50,000, convergence tolerance=0.0000100, radius of effect=65.000000 nm, relative permittivity=12.900000, clock high=9.800000e−022 J, clock low=3.800000e−023 J, clock shift=0, clock amplitude factor=2.000000, layer separation=11.500000 and maximum iterations per sample=100. Most of the mentioned parameters are default values in QCADesigner.

Figs. 11 and 12 show simulation results of proposed five-input majority gate and one-bit full-adder is constructed using this new device.

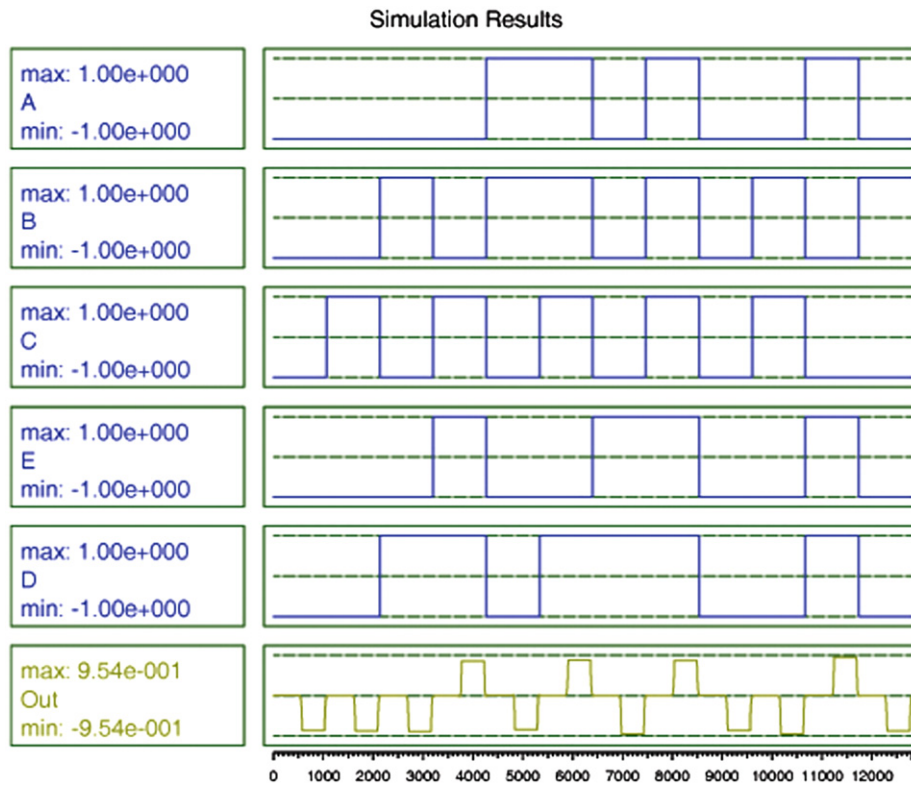


Fig. 11. Simulation results for proposed five-input majority gate.

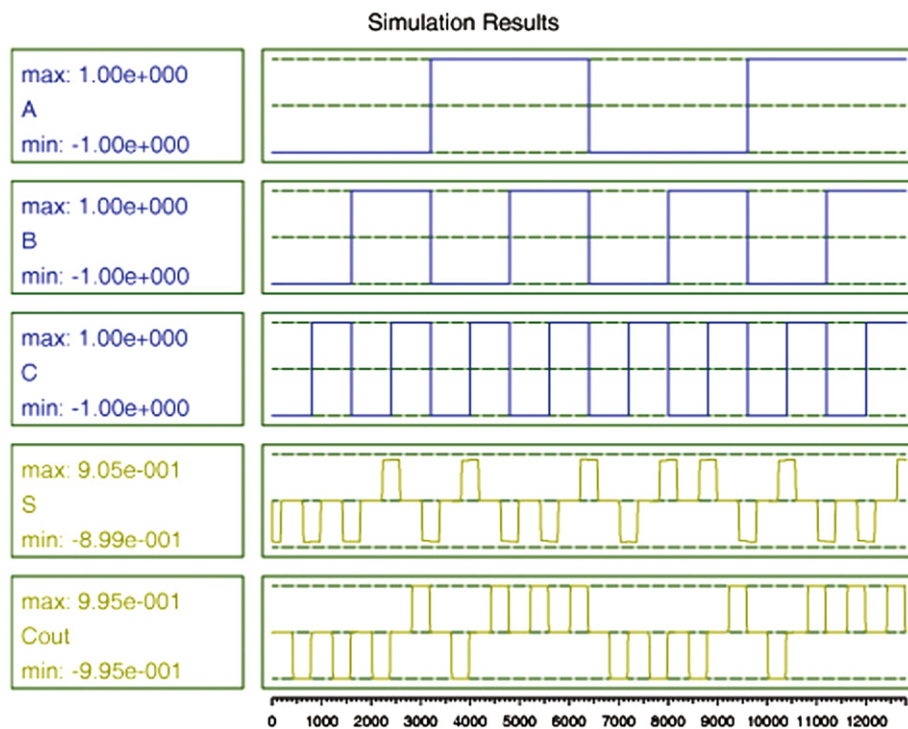


Fig. 12. Simulation results for proposed one-bit full-adder.

Layout of the previous designs and their simulation results are prepared and compared in this section. Simulation results reveal that the proposed full-adder cell is better than previous ones. Several studies about multilayer design in QCA have been proposed [25,26]. In the traditional QCA design, cells are placed on a single plane, but

in the proposed design we used multilayer interconnection by stacking cells one on top of another that can transmit signal on another layer. In this paper we applied the inputs on upper layer.

Table 3 demonstrates the differences among all the designs discussed in this paper.

Table 3
Comparison of QCA full-adders.

	Area	Cell count	Delay
Previous design [4]	0.20	192	Not applicable
Previous design [7]	$> 0.9 \times 2$	$> 107 \times 2$	Not applicable
Previous design [14]	0.17	145	5 clock phases
Previous design [15]	0.10	86	3 clock phases
Proposed design	0.04	73	3 clock phases

5. Conclusion

A novel expandable five-input majority gate for quantum-dot cellular automata and a new full-adder cell are presented. Utilizing this five-input majority gate high performance logic component can be achieved. This majority device is designed using only 10 QCA cells and is fully expandable. In order to illustrate usefulness of this five-input majority function a new QCA full-adder has been implemented. The new full-adder has significant improvements in comparison to state-of-the-art full-adders in terms of area and complexity and has a similar delay to the fastest previous design.

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